

MODEL NAME : ZBW00  
PCB NO :

# Dell / Compal Confidential

## Schematic Document

### Intel Bay Trail M

### OAK MLK UMA

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X76@ : 76 level  
46@ : 46 level  
3VLP@For EC +3VLP  
EMC@Pop EMC Component  
ESD@Pop ESD Component  
XDP@XDP Component

CONN@Connector Component  
@Un-pop Component  
GCLK@For Green CLK function  
JP@Jump Component  
N3VLP@For EC +3VALW  
NEMC@Un-pop EMC Component  
NESD@Un-pop ESD Component  
TEST@Test Point  
TOUCH@For Touch Screen Function

N2910@CPU Component  
N3510@CPU Component  
R1@PCB

2014-03-10

Rev: 2.0

BOM config

LM-43XXXXXXL01:N2910@/3VLP@/EMC@/ESD@/XDP@/3223@/JHP@

LM-43XXXXXXL01:N2910@/3VLP@/EMC@/ESD@/XDP@/3234@/JHP@



PCB ZBW00 LA-B481P LS-9101PI-9103P  
DA216D00100



PCB ZBW00 LA-B481P LS-9101PI-9103P GOLD A31 !  
DA216D00101

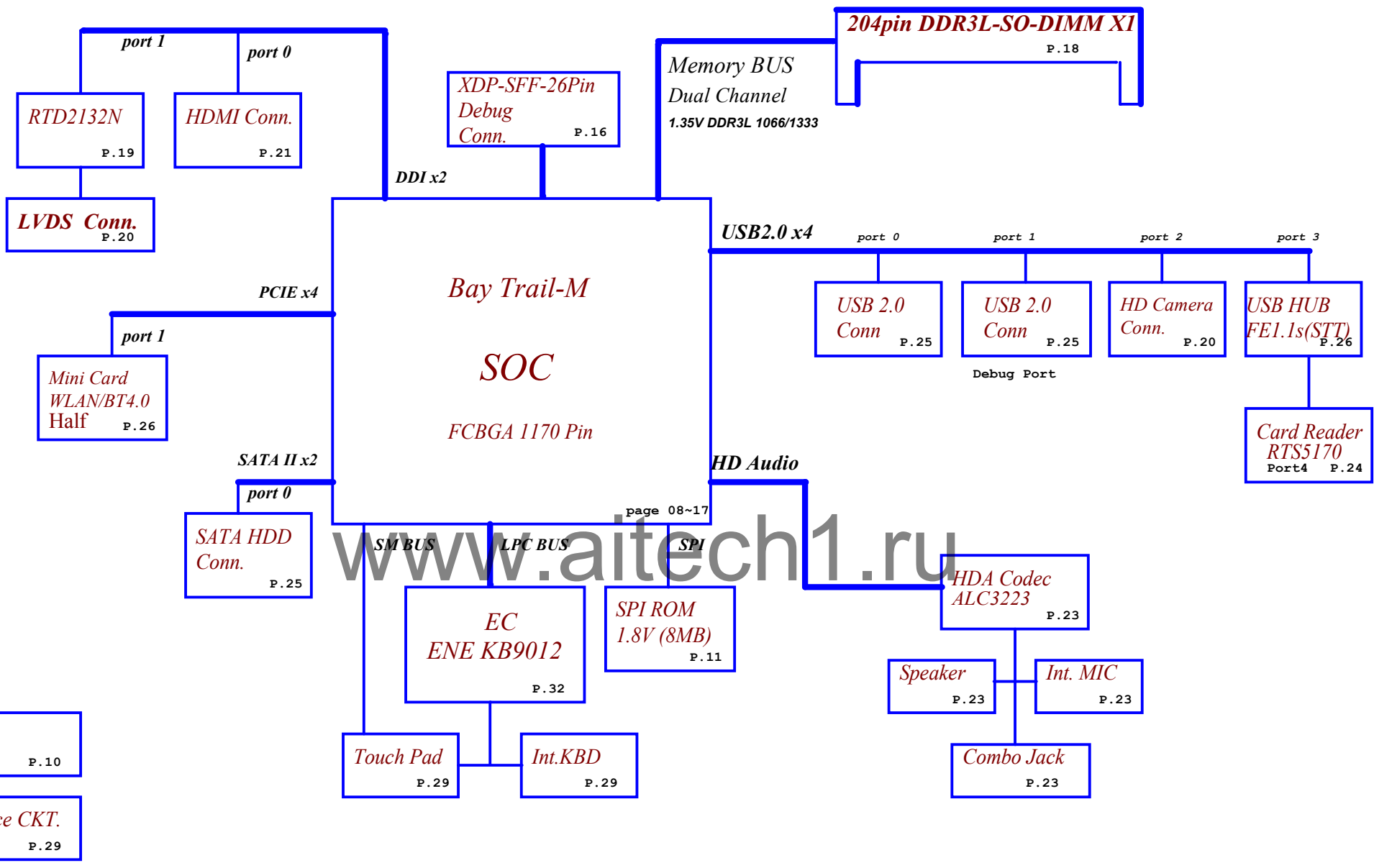


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Part Number = SA00007QR1L



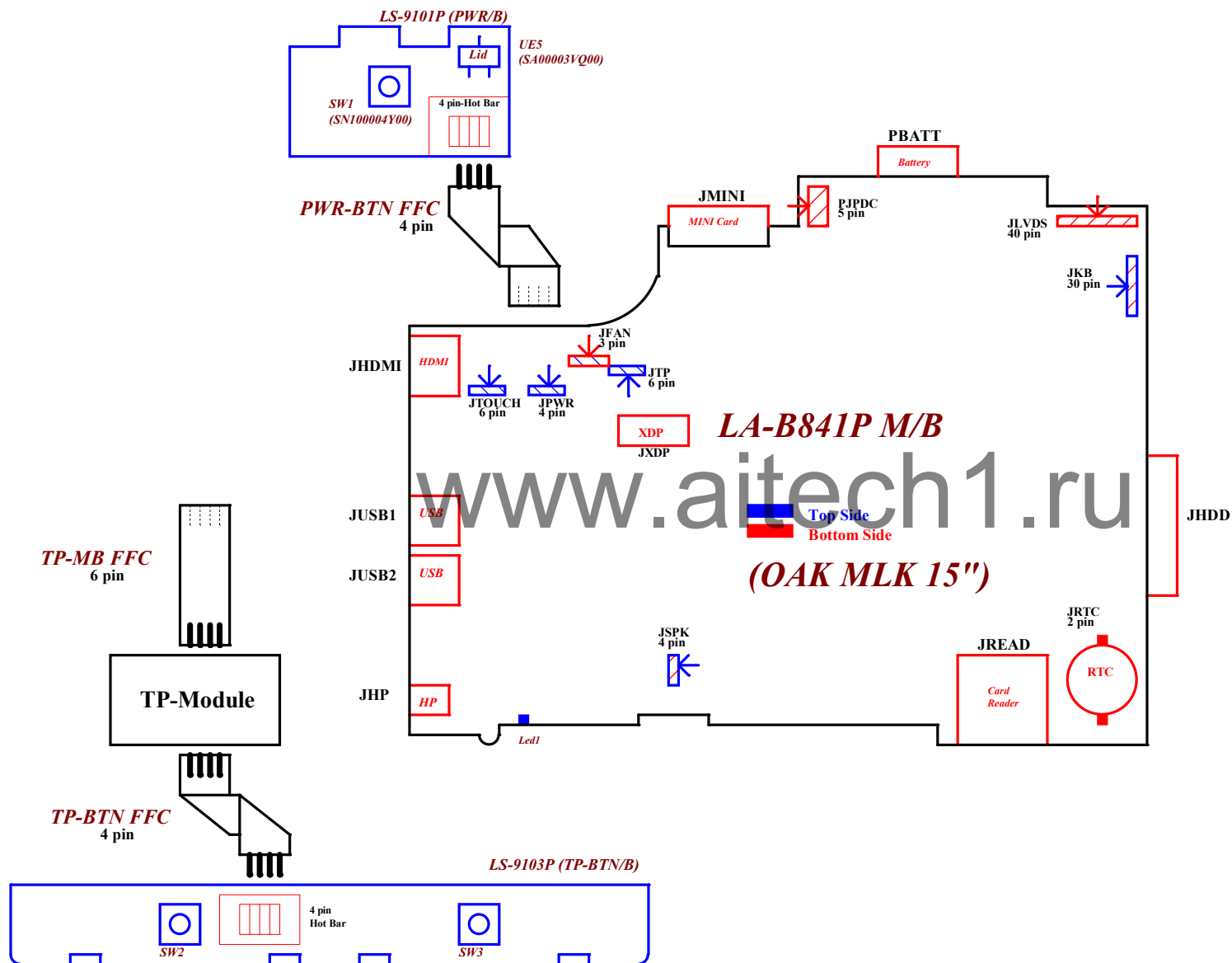
USOC1  
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Part Number = SA00007QR2L

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				2	2.0

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**Project Code : ZBW00**  
**File Name : LA-B841P**



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Voltage Rails

Power Plane	Description	S0	S3	S4/S5
VIN	19V Adapter power supply	ON	ON	ON
BATT+	12V Battery power supply	ON	ON	ON
B+	AC or battery power rail for power circuit. (19V/12V)	ON	ON	ON
+RTCVCC	RTC Battery Power	ON	ON	ON
+1.0VALW	+1.0v Always power rail	ON	ON	ON
+1.8VALW	+1.8v Always power rail	ON	ON	ON
+3VALW	+3.3v Always power rail	ON	ON	ON
+5VALW	+5.0v Always power rail	ON	ON	ON
+1.35V	+1.35V power rail for DDR3L	ON	ON	OFF
+SOC_VCC	Core voltage for SOC	ON	OFF	OFF
+SOC_VNN	GFX voltage for SOC	ON	OFF	OFF
+0.675VS	+0.675V power rail for DDR3L Terminator	ON	OFF	OFF
+1.0VS	+1.0v system power rail	ON	OFF	OFF
+1.05VS	+1.05v system power rail	ON	OFF	OFF
+1.35VS	+1.35v system power rail	ON	OFF	OFF
+1.5VS	+1.5v system power rail	ON	OFF	OFF
+1.8VS	+1.8v system power rail	ON	OFF	OFF
+3VS	+3.3v system power rail	ON	OFF	OFF
+5VS	+5.0v system power rail	ON	OFF	OFF
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.				

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	X01
1	X02
2	X03
3	A00
4	
5	
6	
7	

BOM Option Table

Item	BOM Structure
Unpop	@
Connector	CONN@
XDP (Debug Port)	XDP@
EMC requirement	EMC@
EMC requirement unpop	@EMC@
TPM	TPM@
Touch Screen	TS@
R short	RS@
Test Point	TEST@

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
SOC SM Bus address	
Device	Address
SO-DIMM A (JDIMM1)	A0h

EC SM Bus2 address

Device	Address
SoC	0x9A
MINI Card	0x98
DDR	0x82
RTD2136	0x94

43 level BOM table

43 Level	Description	BOM Structure
4319T731L01	SMT MB AB481 ZBW00 UMA BTM HDMW2R30R1@/EMC@/ESD@/XDP@/3223@/JHP@/R1@	

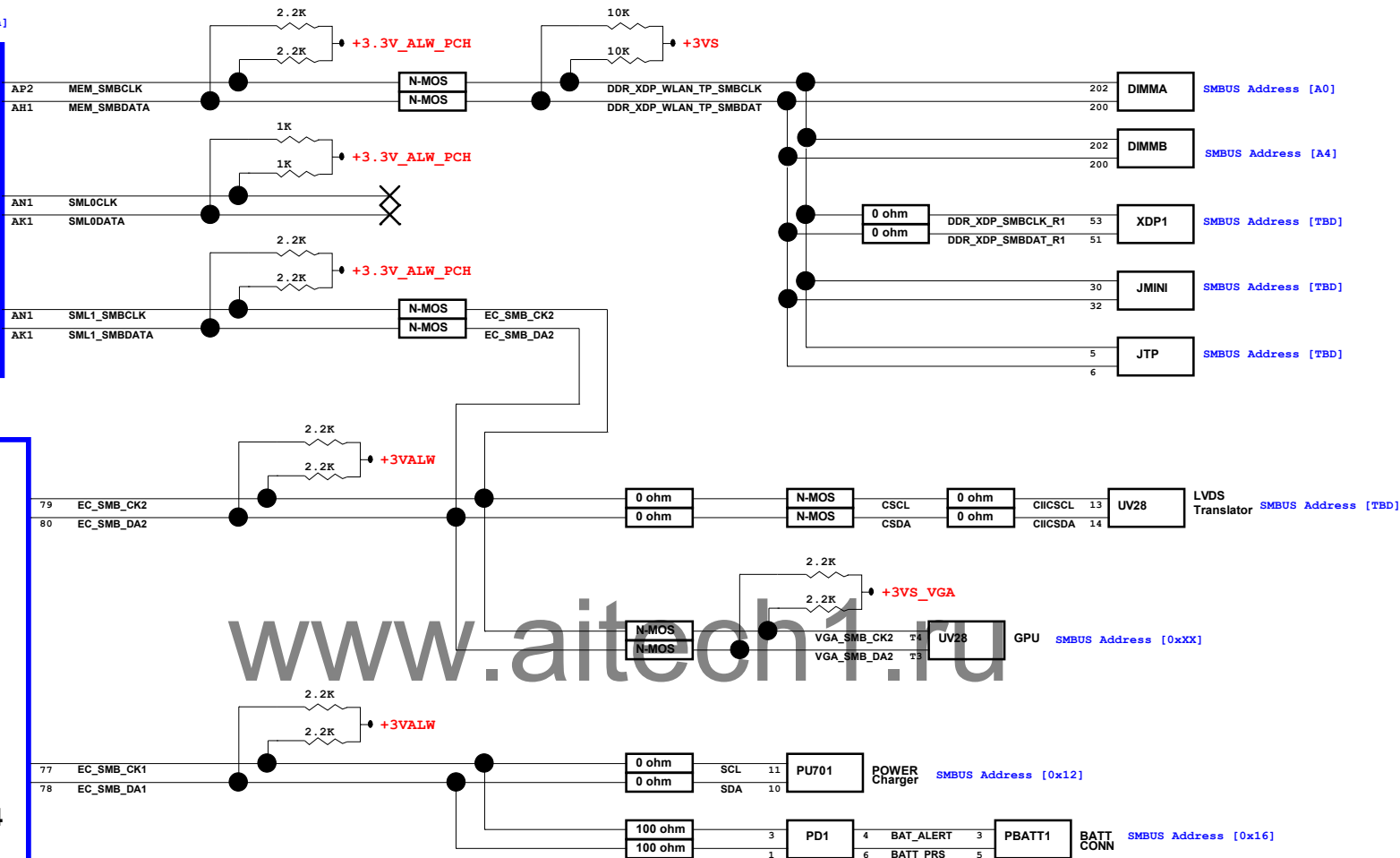
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SMBUS Address [0x9a]

MCH  
Shark bay

KBC  
KB9012A4



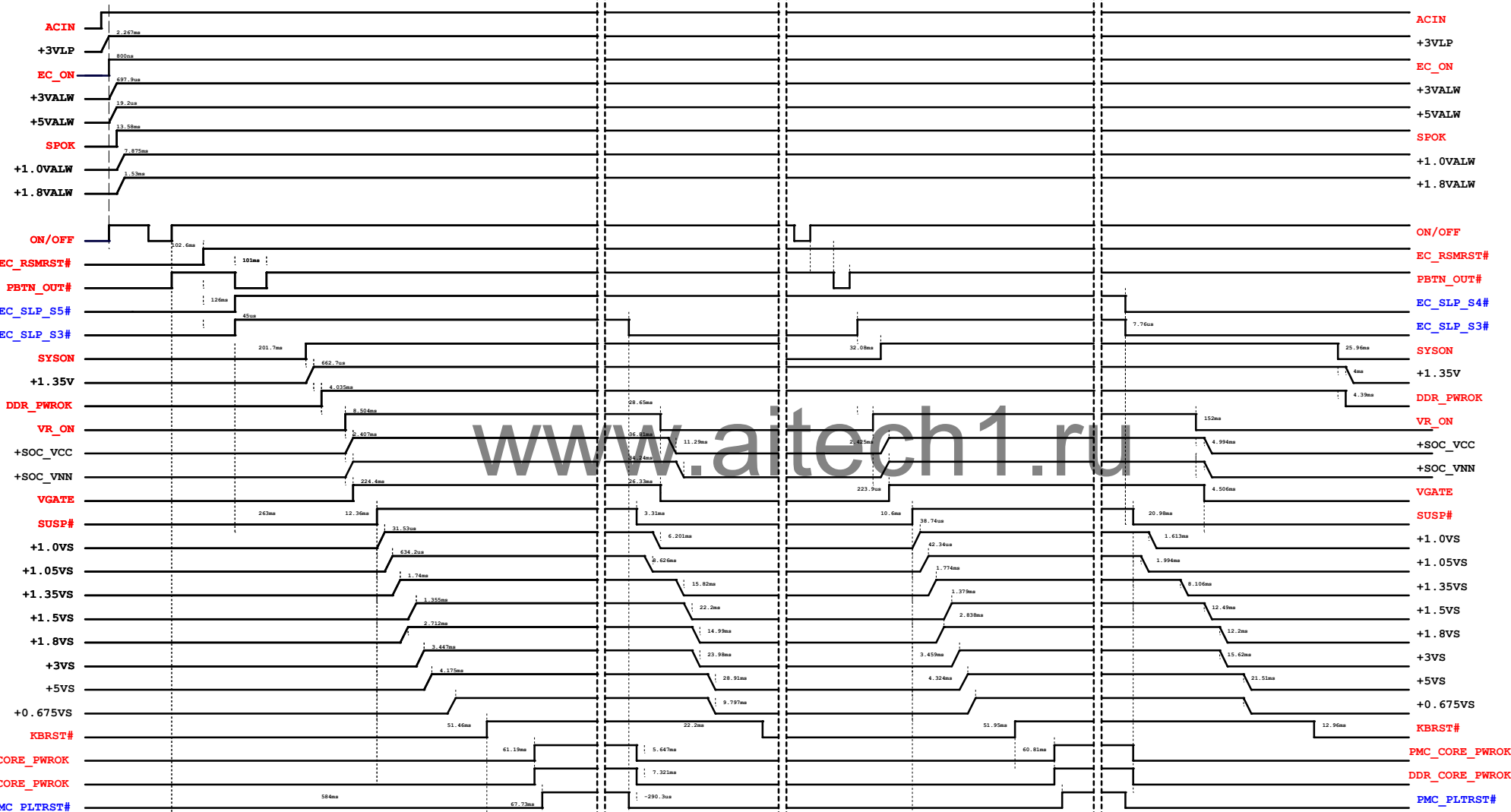
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S5-&gt;S0

S0-&gt;S3

S3-&gt;S0

S0-&gt;S5

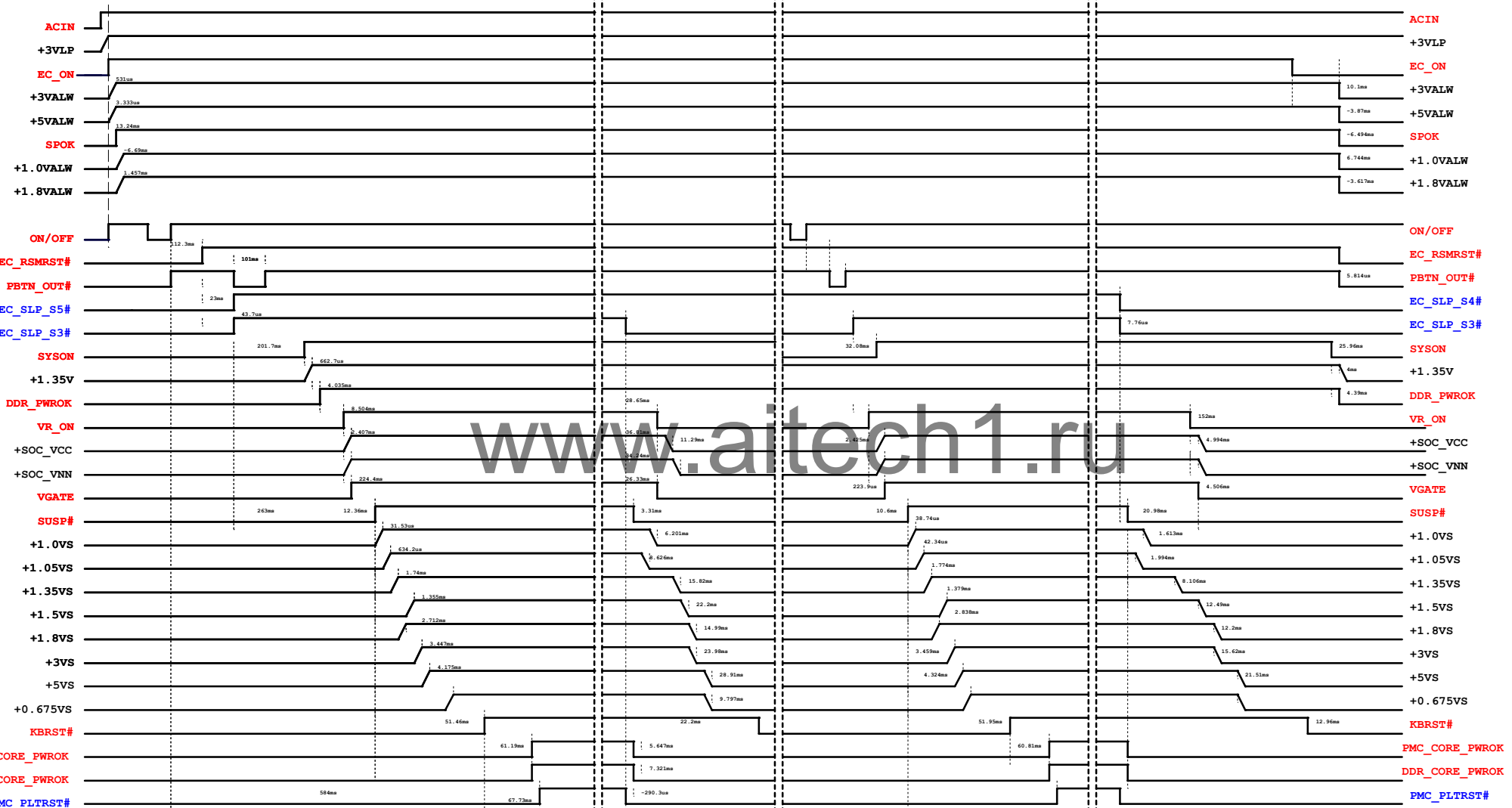


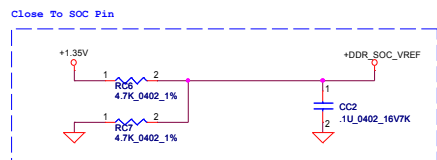
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S0-&gt;S3

S3-&gt;S0

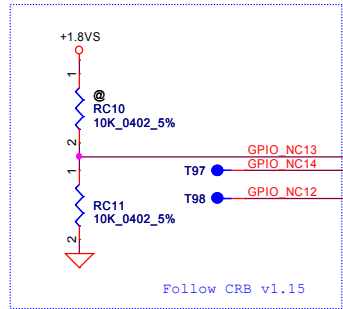
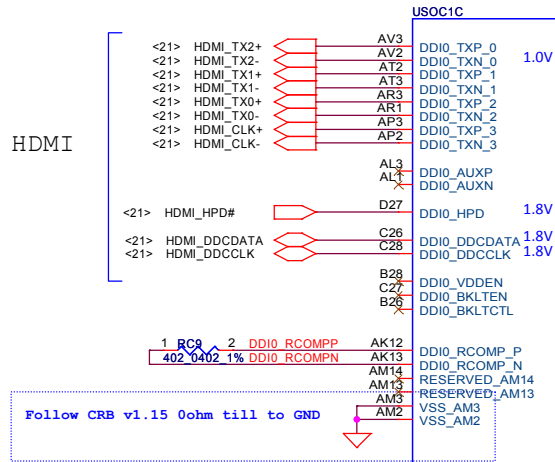
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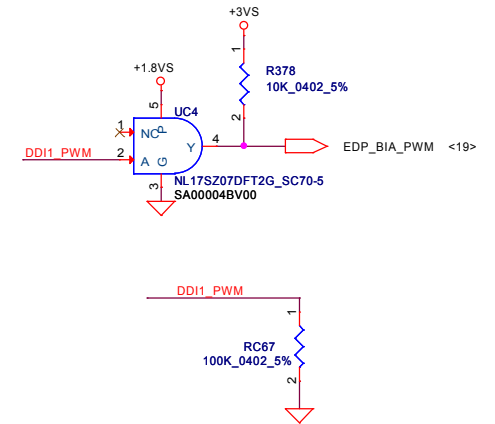
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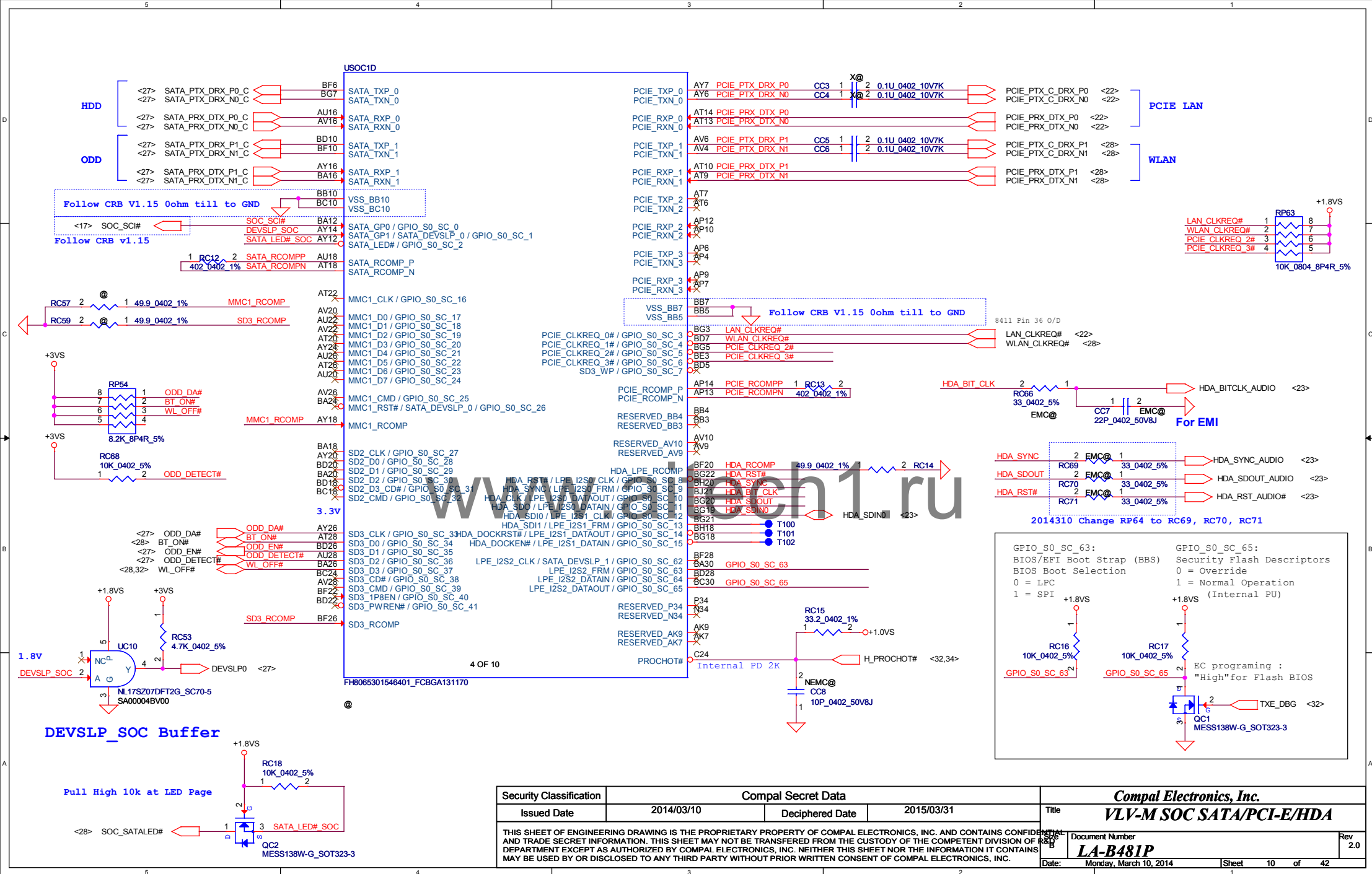
3 OF 10



eDP to LVDS Panel



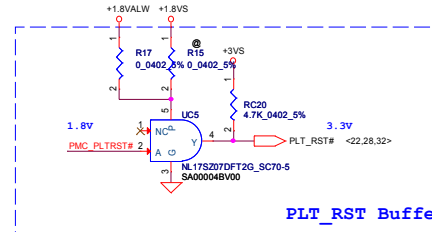
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		Size	Document Number	Rev	
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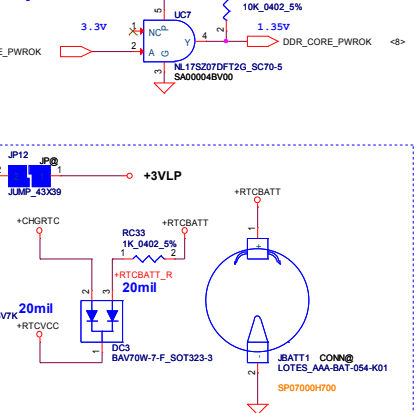
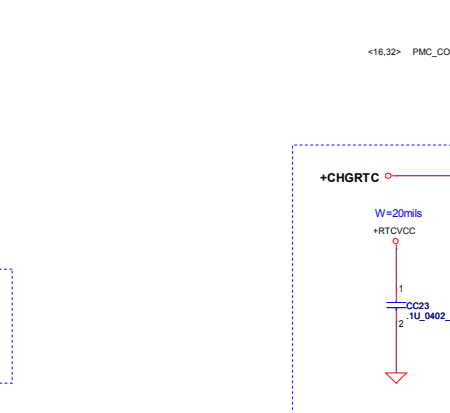
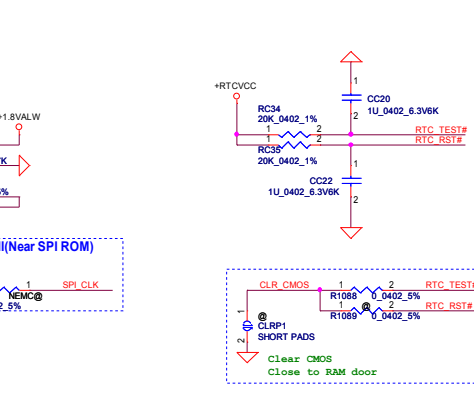
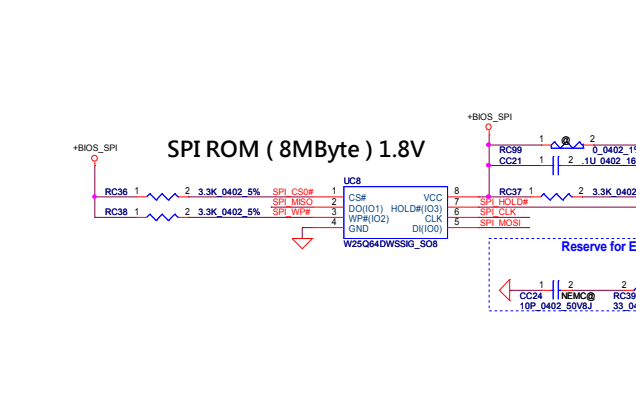
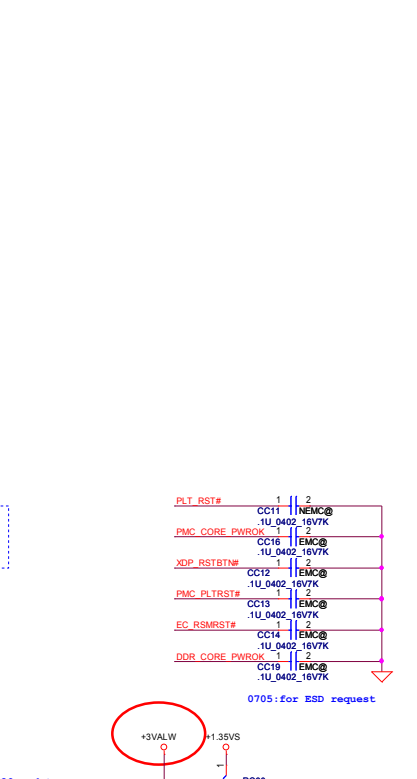
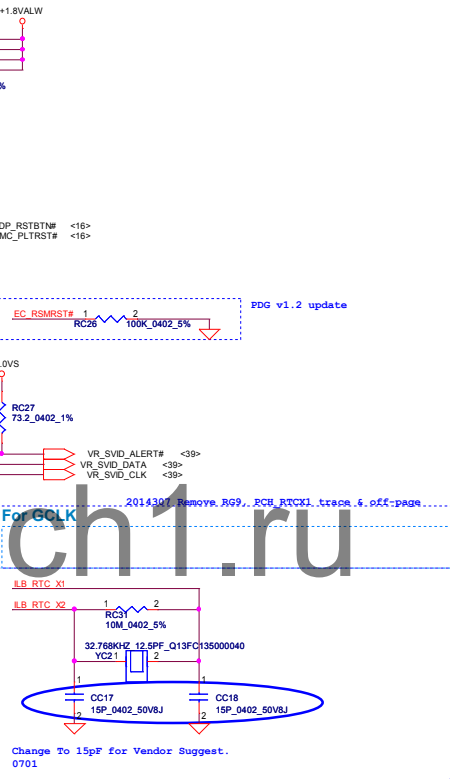
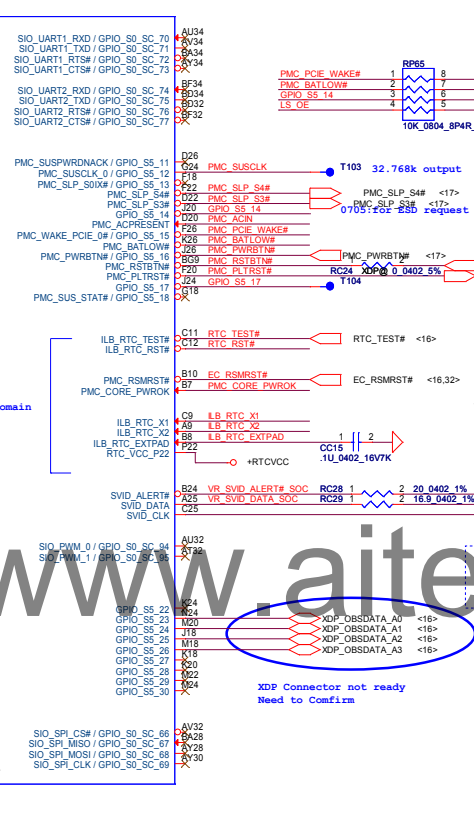
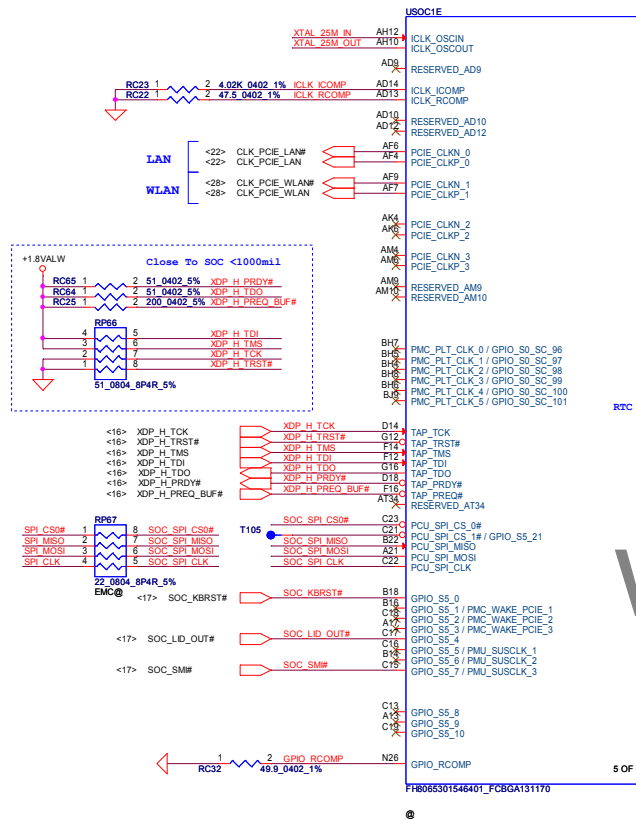
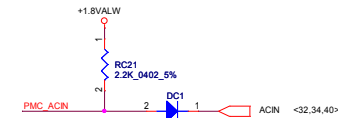
Change To 10pF for Vendor Suggest.  
0701

### For GCLK

<31> PCH\_X1



### PLT\_RST Buffer

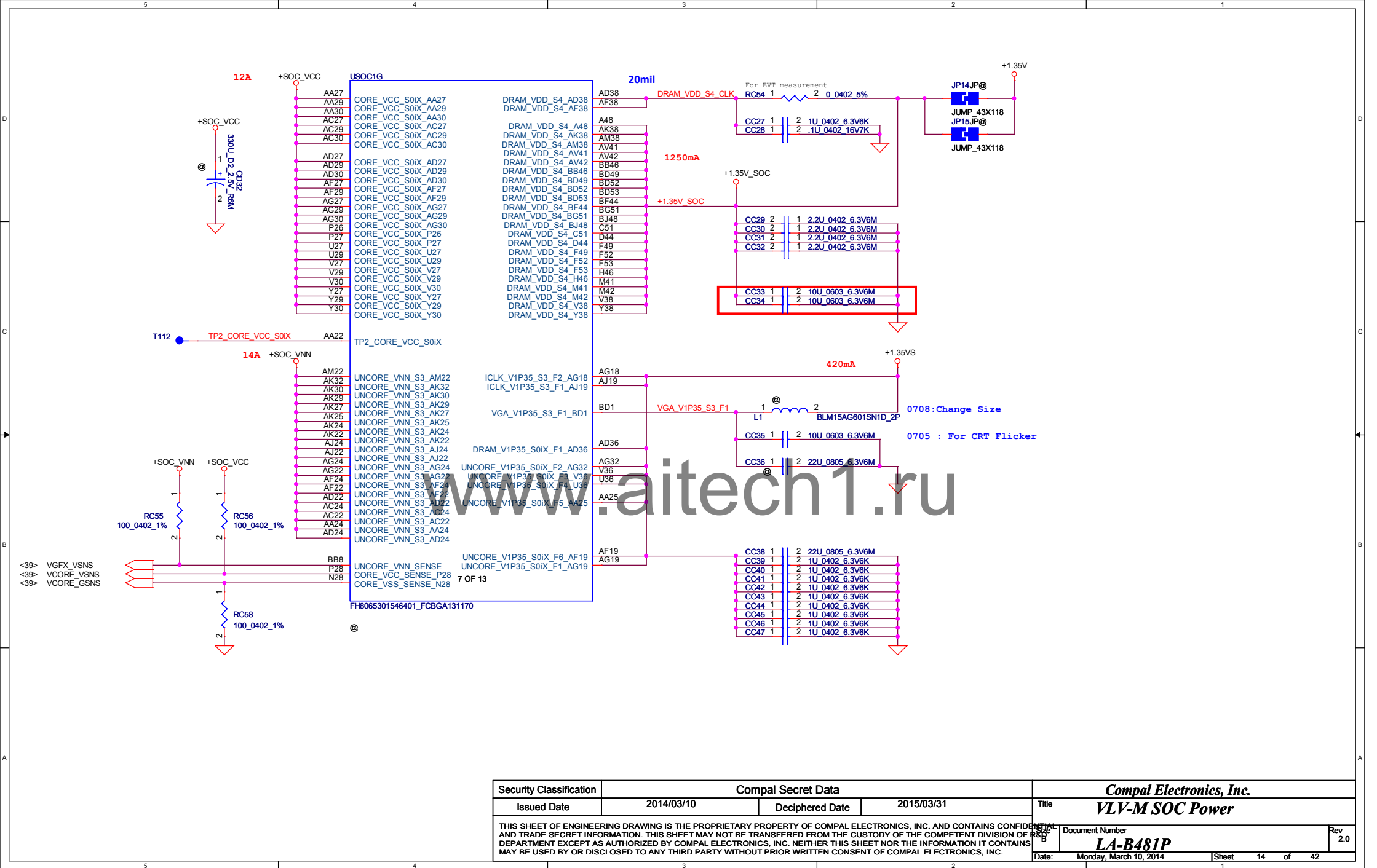


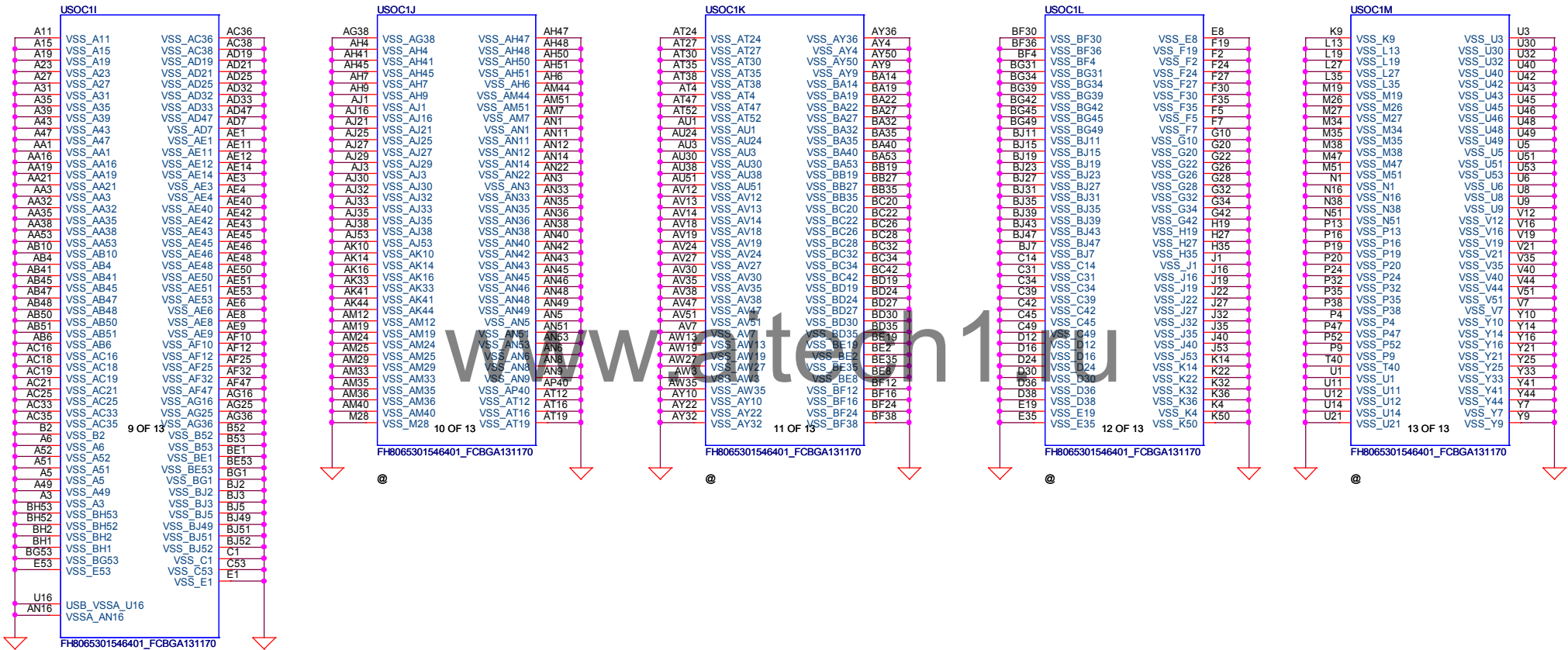
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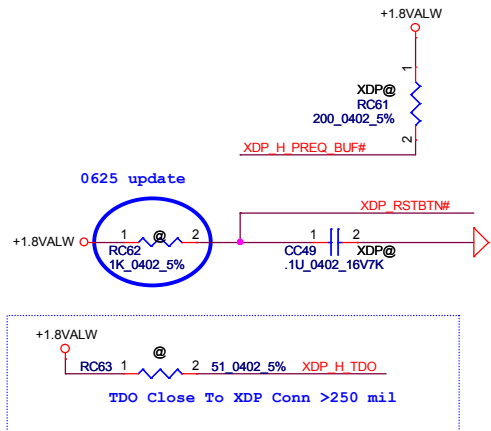




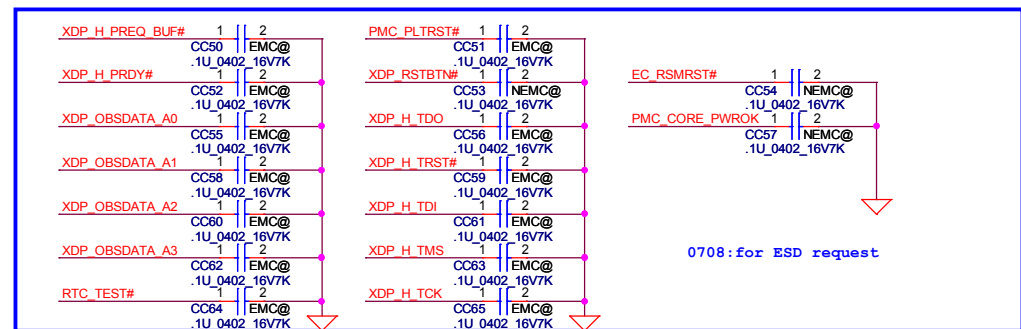
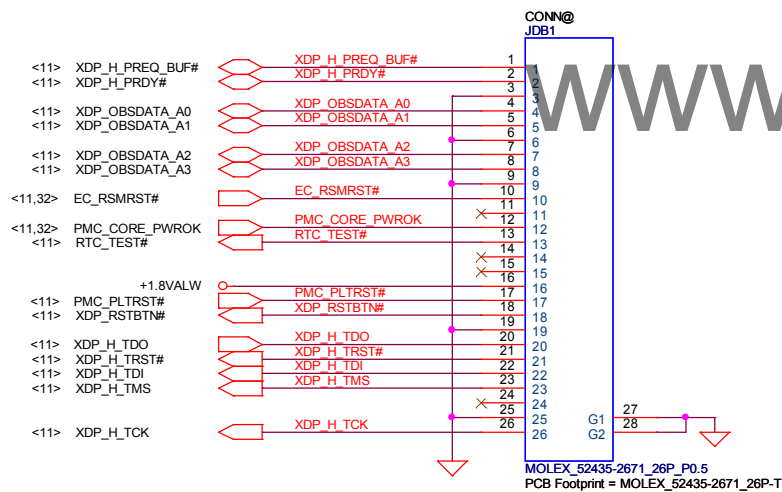




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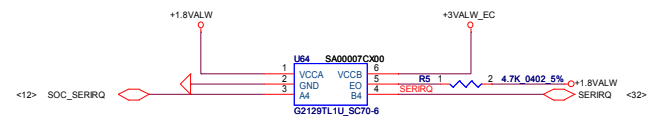
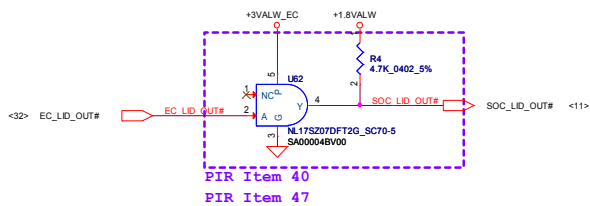
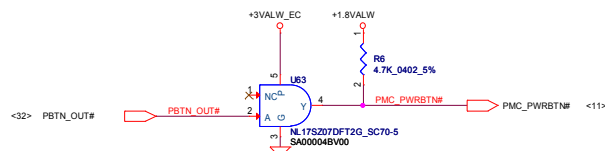
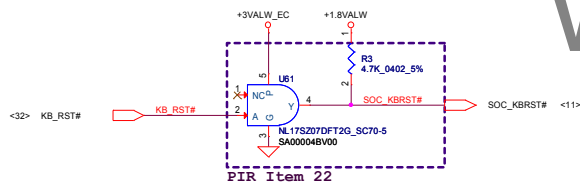
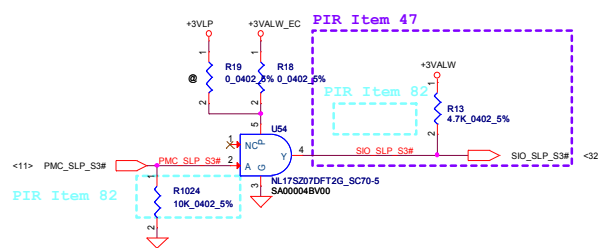
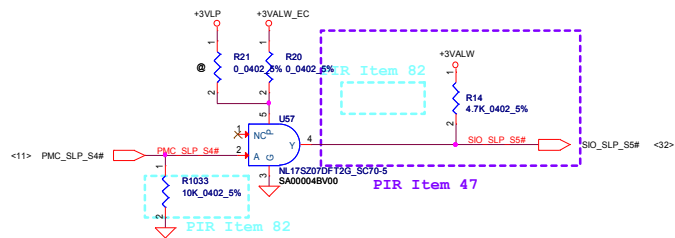
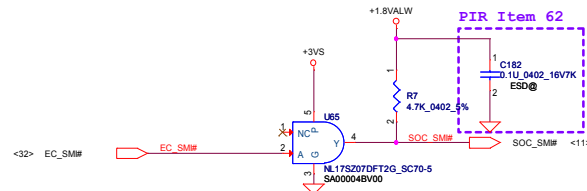
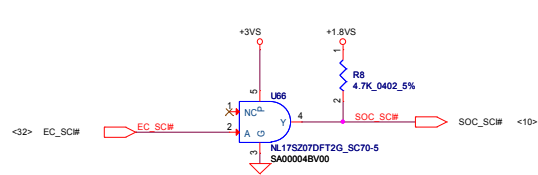


## XDP-SFF-26Pin



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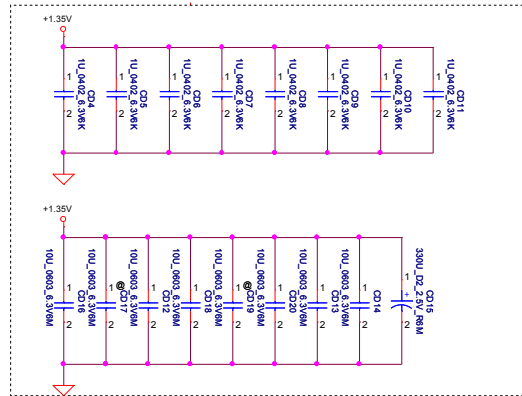
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Populate RD1, De-Populate RD7 for Intel DDR3  
VREFDQ multiple methods M1  
Populate RD7, De-Populate RD1 for Intel DDR3  
VREFDQ multiple methods M3

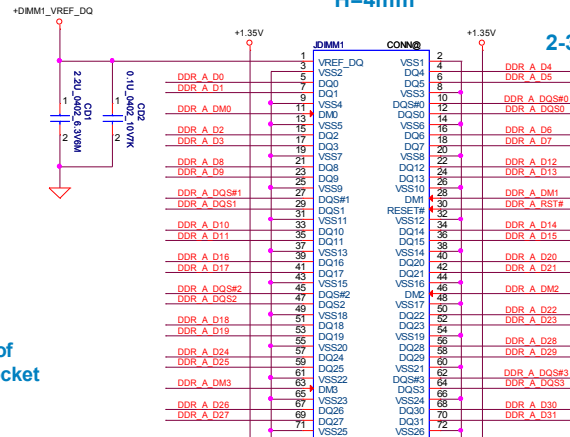
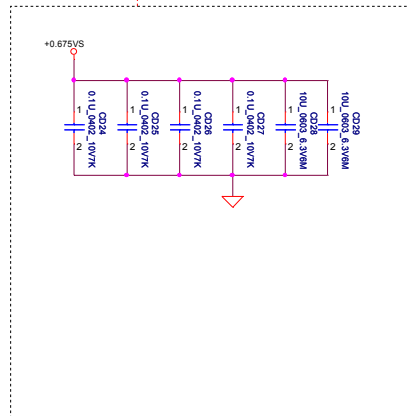
<-> DDR\_A\_DM[0..7]  
<-> DDR\_A\_DQS[0..7]  
<-> DDR\_A\_DQ[0..63]  
<-> DDR\_A\_DQS[0..7]  
<-> DDR\_A\_MA[0..15]

Layout Note:  
Place near JDIMM1

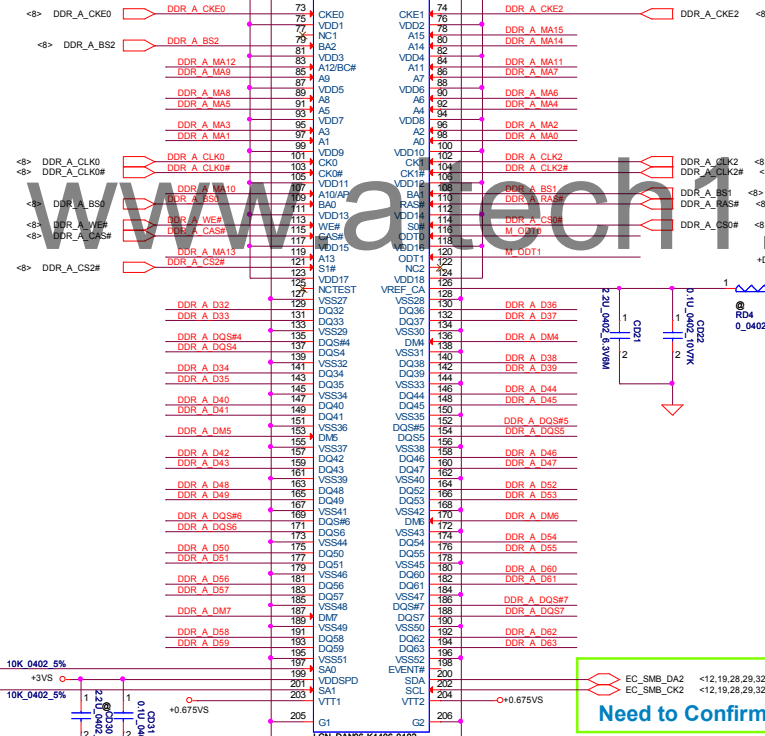
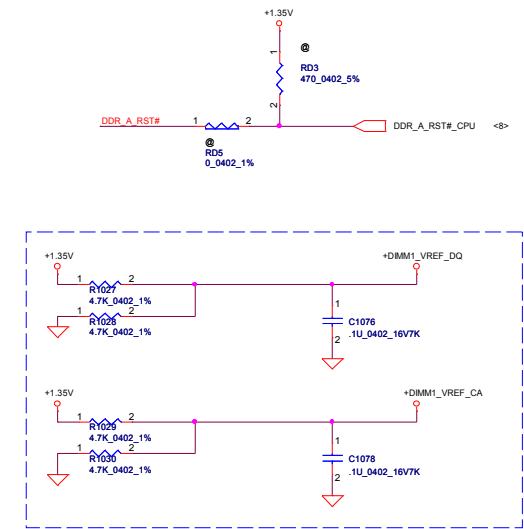
Note:  
Check voltage tolerance of  
VREF\_DQ at the DIMM socket



Layout Note:  
Place near JDIMM1.203,204



CAD NOTE  
PLACE THE CAP NEAR TO  
DIMM RESET PIN



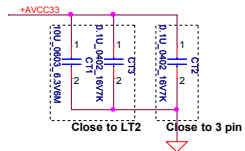
Need to Confirm

Channel A

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DIMM\_1 STD H:4mm

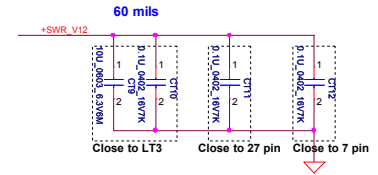
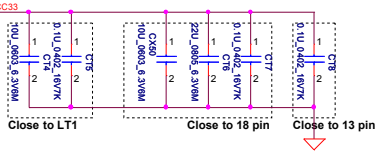


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				Sheet	18 of 42

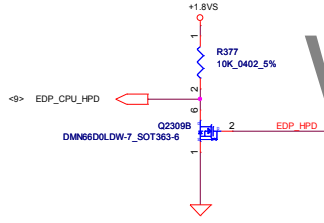
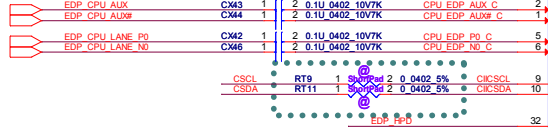


#### Power Consumption:

Pin22 (DPV33) < 20mA  
 Pin 11 (DP\_V12) < 100mA  
 Pin 15 (SWR\_VCC) < 100mA (layout trace > 60 mil)  
 Pin 17 (SWR\_LX) < 600mA (layout trace > 60 mil)  
 Pin 18 (SWR\_VDD) < 200mA (layout trace > 40 mil)  
 Pin 22 (PVCC) < 50 mA  
 Pin 43 (VCC) < 50mA



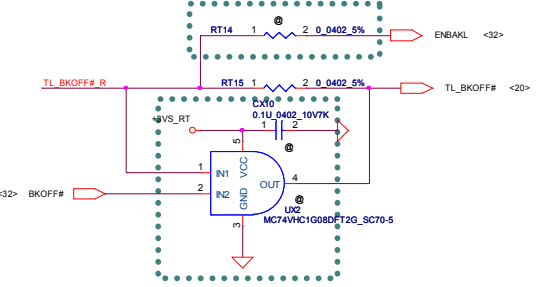
<9> EDP\_CPU\_AUX  
 EDP\_CPU\_AUX#  
 <9> EDP\_CPU\_LANE\_P0  
 EDP\_CPU\_LANE\_N0



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RTD2132R : SA000069200  
 RTD2132N : SA00007A300

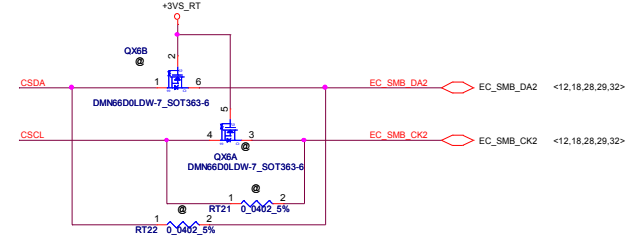
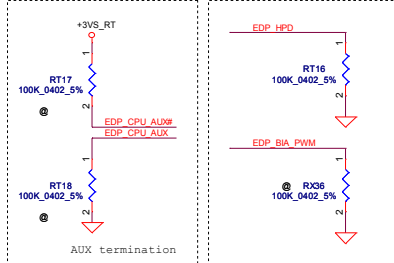
#### Vendor advise reserve it



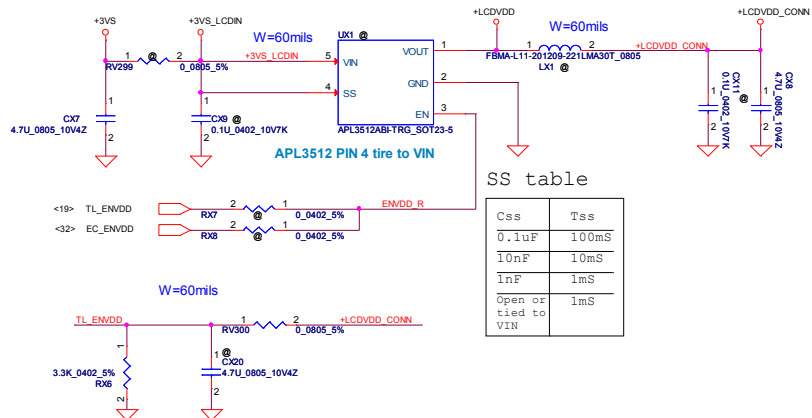
Pull-Down 100K

1: RevD W EEPROM  
 0: RevE W/O EEPROM

		Pin47 MIIC_SDA	
		0	1
Pin48 MIIC_SCL	0	x	EP MODE
	1	ROM	EEPROM

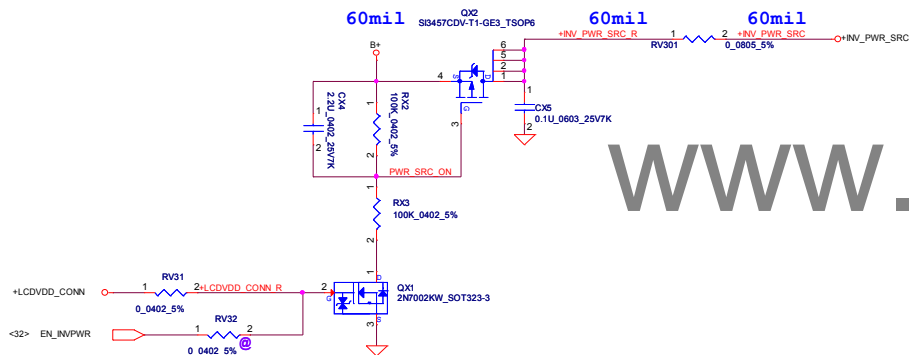


## LCD PWR CTRL

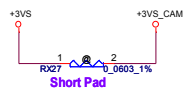


Css	Tss
0.1uF	100mS
10nF	10mS
1nF	1mS
Open or tied to VIN	1mS

## LCD backlight PWR CTRL

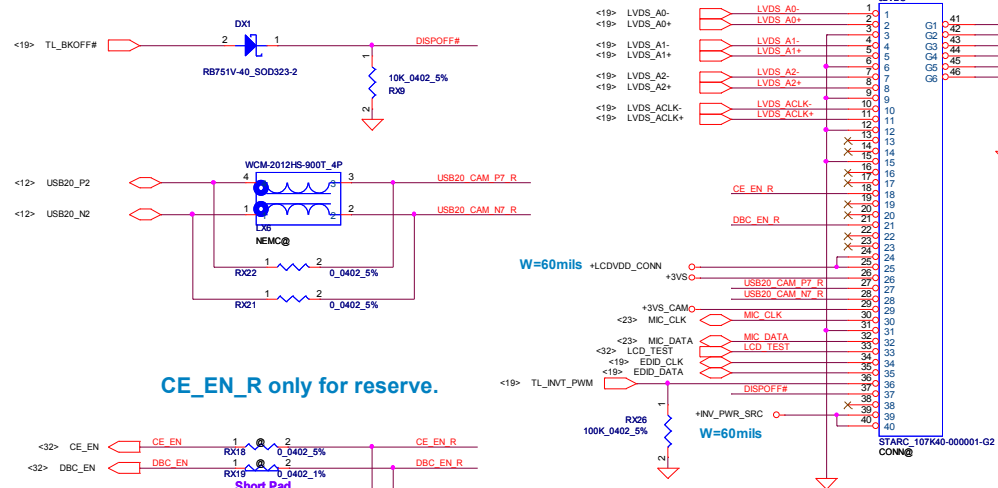


## Webcam PWR CTRL

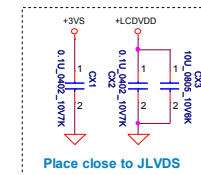
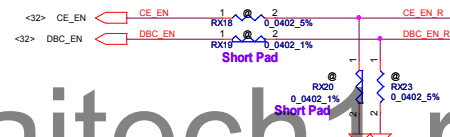


Short pad list  
RX19  
RX27

## LVDS Connector



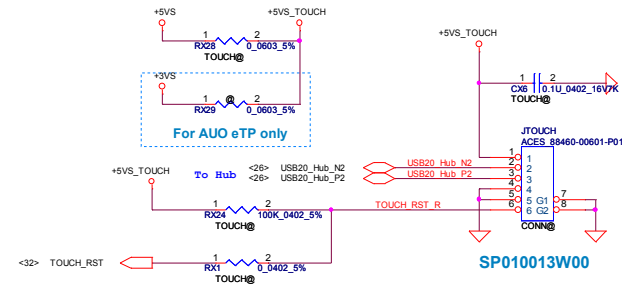
CE\_EN\_R only for reserve.



Place close to JLVDS

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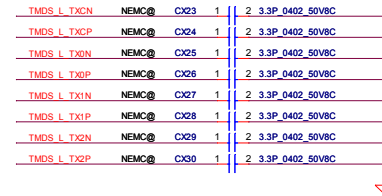
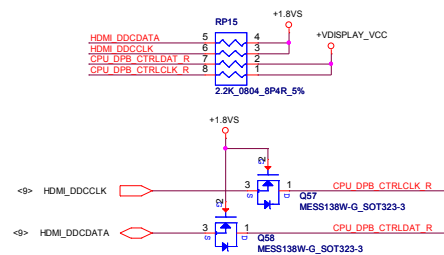
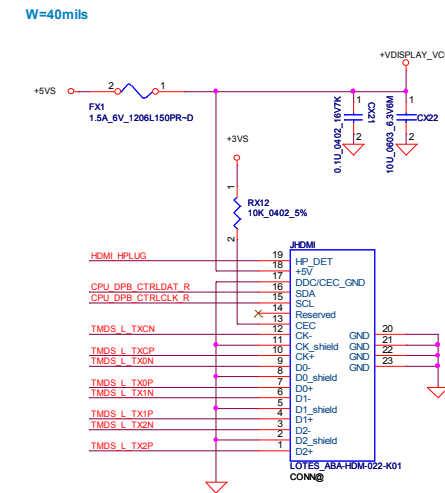
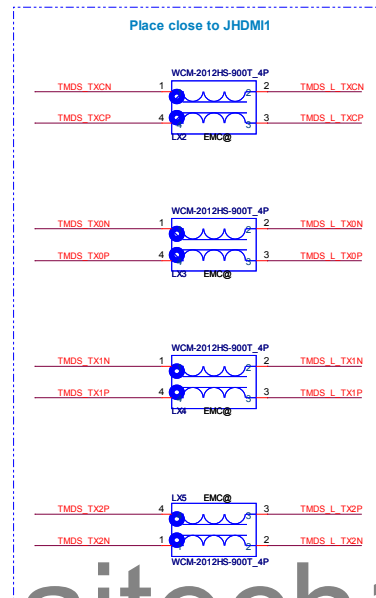
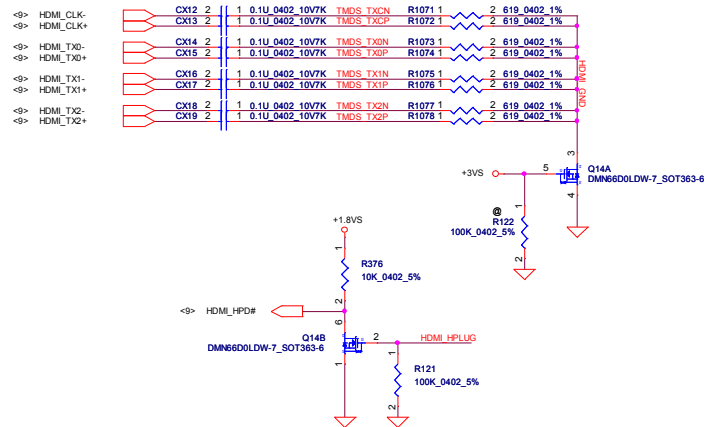
**\* Touch Screen Panel**



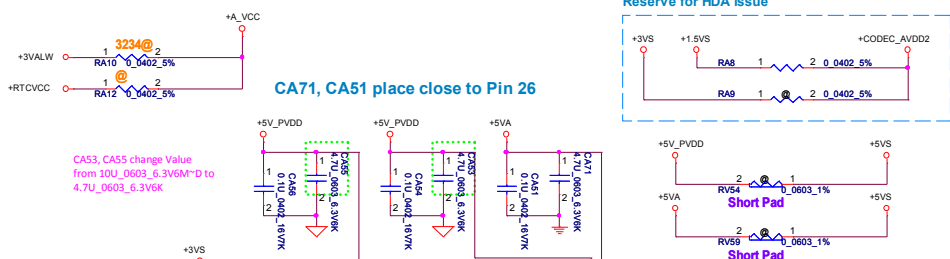
**OAK 15 only**

Security Classification	Compal Secret Data			<b>Compal Electronics, Inc.</b>		
Issued Date	2014/03/10	Deciphered Date	2015/03/31	Title <b>LVDS/webcam/touch</b>		
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					<b>LA-B481P</b>	<b>2.0</b>
Date: Monday, March 10, 2014				Sheet	20	of 42







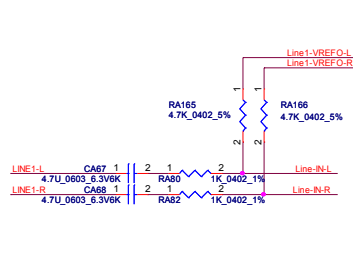
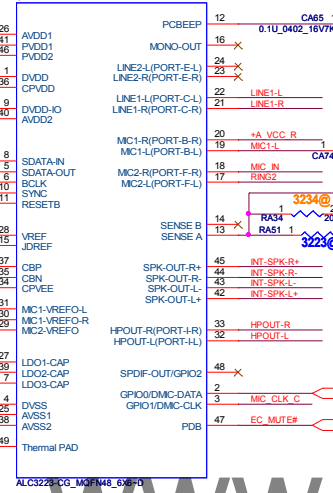
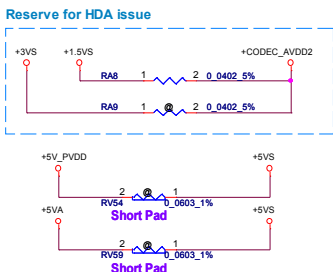


CA57,CA58 close to UA1 pin1

Digital power for HDA link (Bay Trail M -- Pin9 -->1.5VS)

100K is used to speed up the discharge for LDO1. It could solve the pop sound during system boot up and reboot. RA154 place close to Pin 26

RA154 Reserve for ESD Request

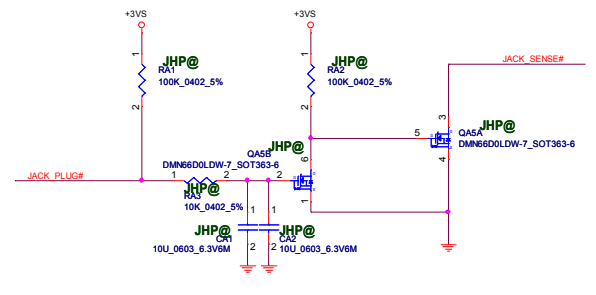


PCB trace width of SLEEVE & RING2 are required at least 40 mil and its length should be as short as possible.

RA155 Reserve for ESD Request

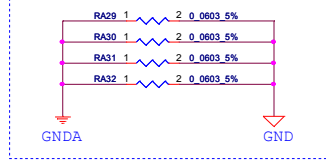
RA51, RA33 place close to UA1

### JACK\_PLUG Delay circuitis

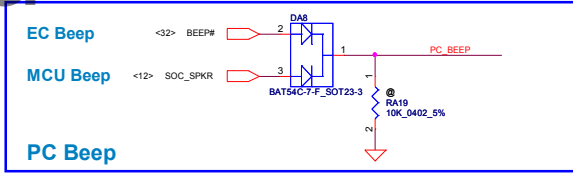


### Reserve for cancel Delay circuitis

Change to 0 ohm from short pad



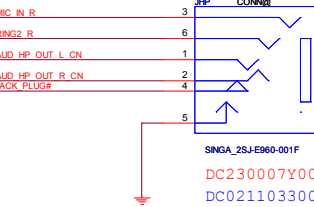
Place on the moat between GND & GNDA.



Close to UA1 Pin11,13,14,16

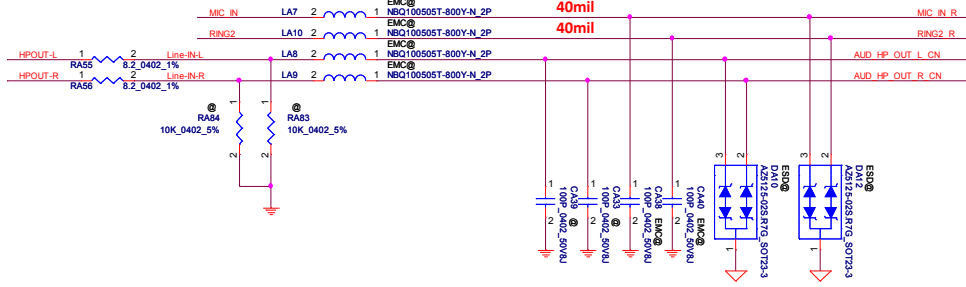
close to Codec

Trace width for SPK-L/SPK-L/SPK-R/SPK-R-Speaker 4 ohm : 40mil Speaker 8 ohm : 20mil

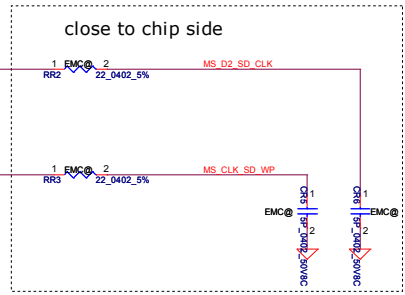
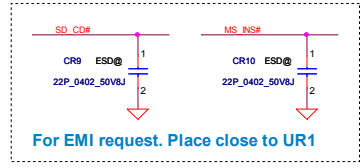
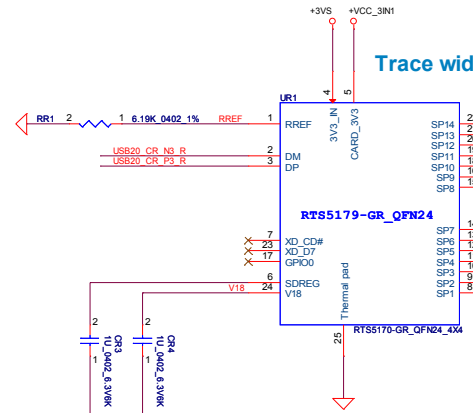
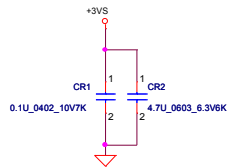
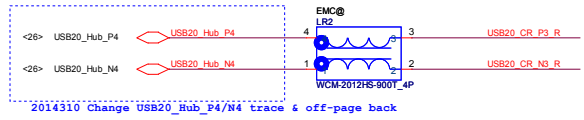


RA57, RA58 Reserve for ESD Request

iPhone type Combo Jack



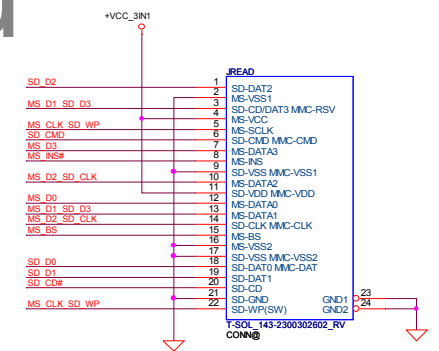
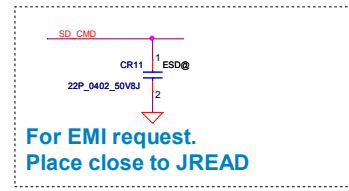
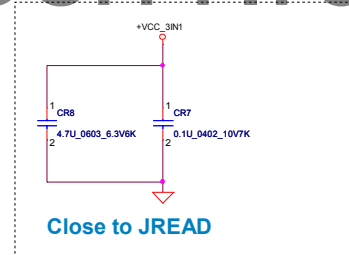
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				LA-B481P	Rev 2.0
				Date:	Monday, March 10, 2014
				Sheet	23 of 42

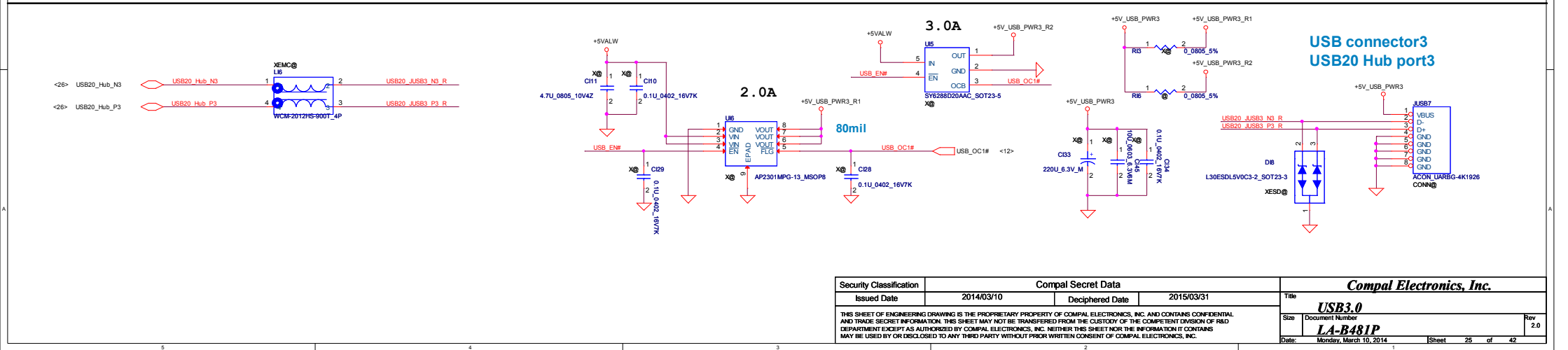
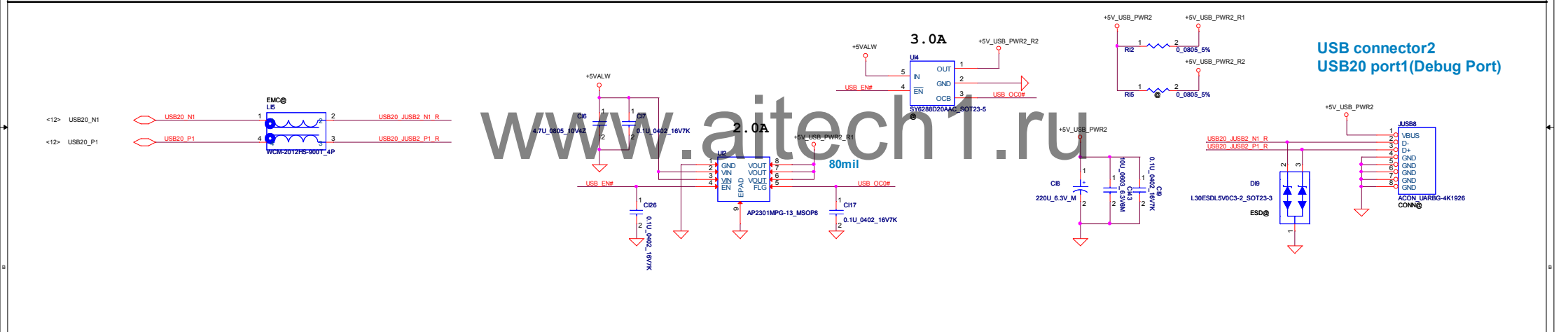
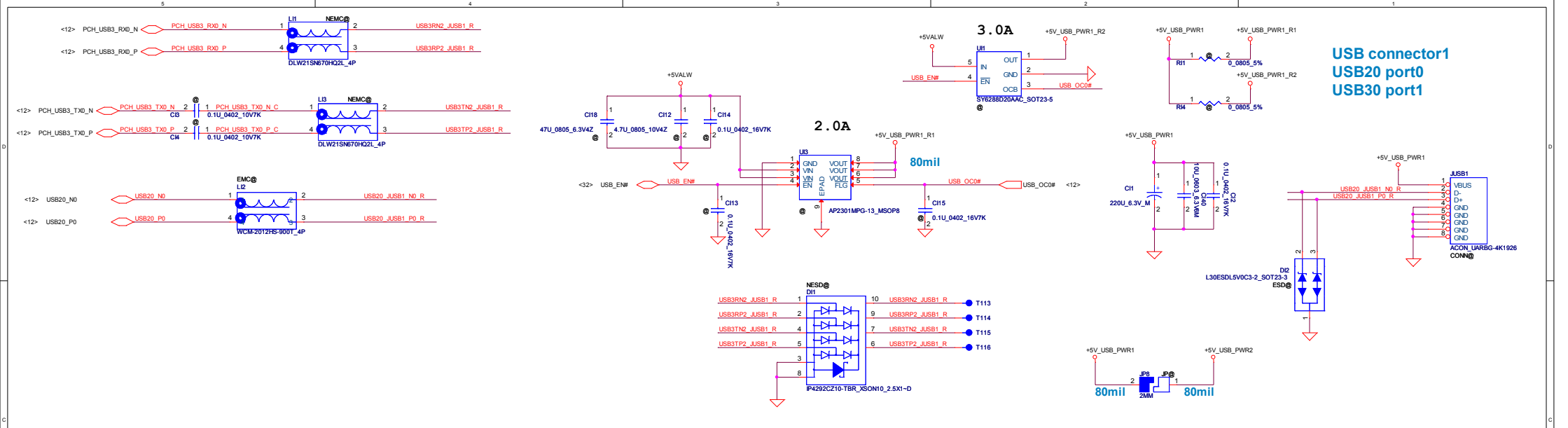


拉MS\_D2\_SD\_CLK到Conn pin 14 SD\_CLK  
 再打Via拉到pin 10 MS\_D2

拉MS\_CLK\_SD\_WP到Conn pin 5 MS\_CLK  
 再打Via拉到pin 22 SD\_W

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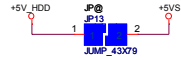




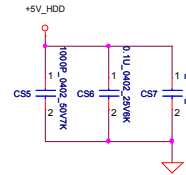
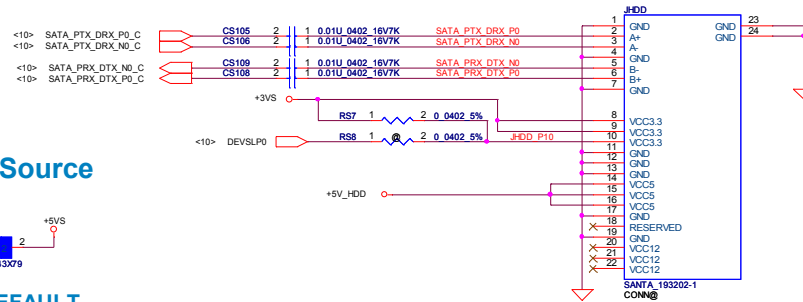


## SATA HDD Connector

### +5V\_HDD Source



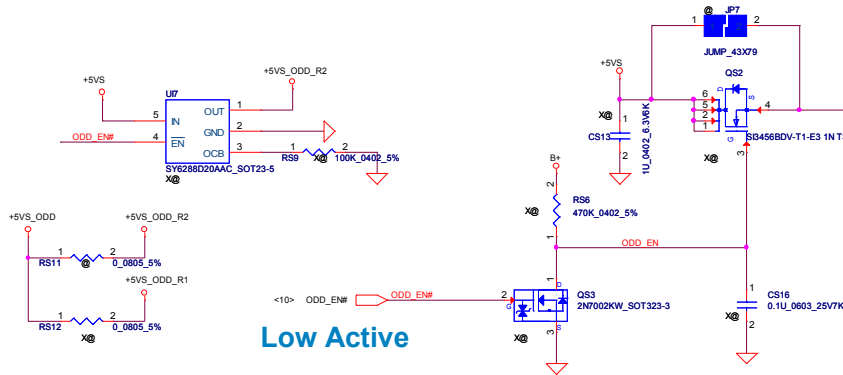
### SHORT DEFAULT



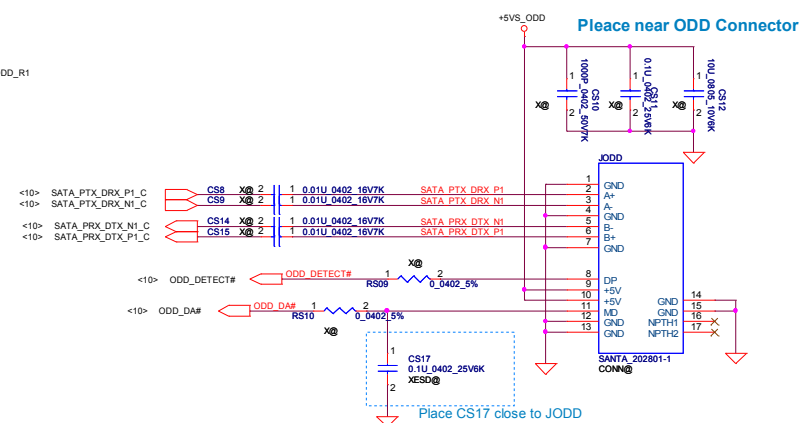
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## ODD Power Control

## SATA ODD Connector

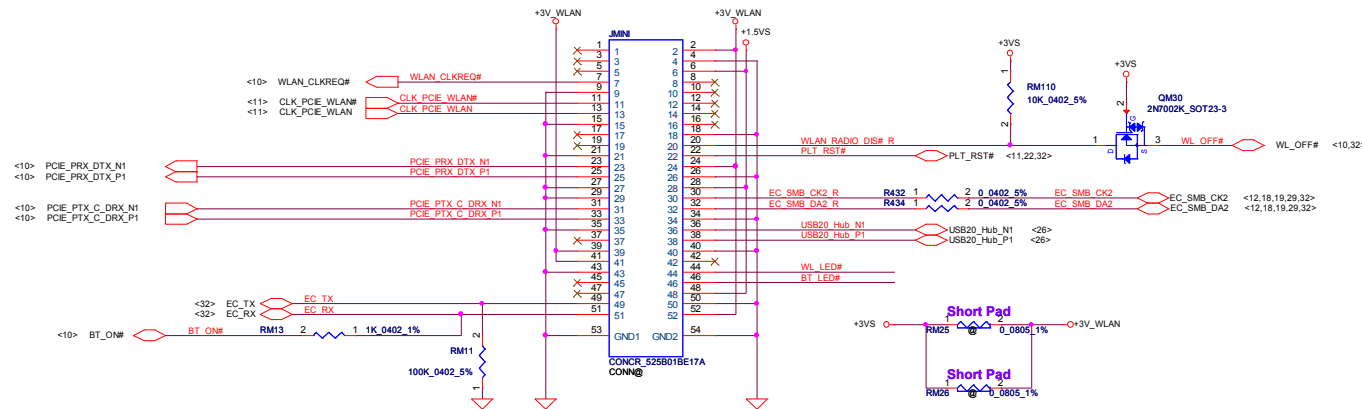


### Low Active



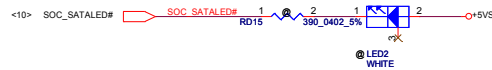
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Issued Date	2014/03/10	Deciphered Date	2015/03/31	Title	HDD/ODD
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# Mini WLAN/WIMAX H=6.7



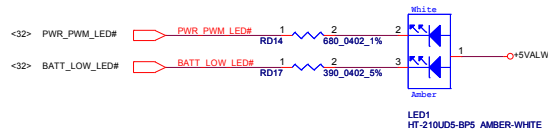
10mils, All pins

## HDD LED

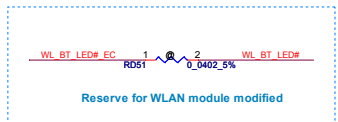
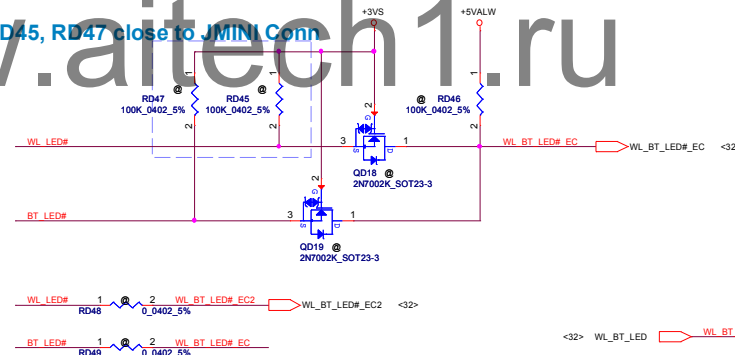


12-21C-T3D-CM2P1B18X-2C\_WHITE

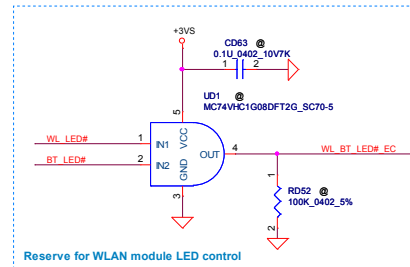
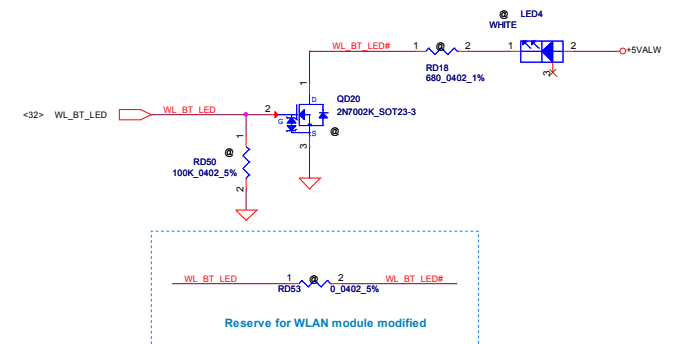
## Power / Battery LED



## RD45, RD47 close to JMIN Conn



## Wireless LED

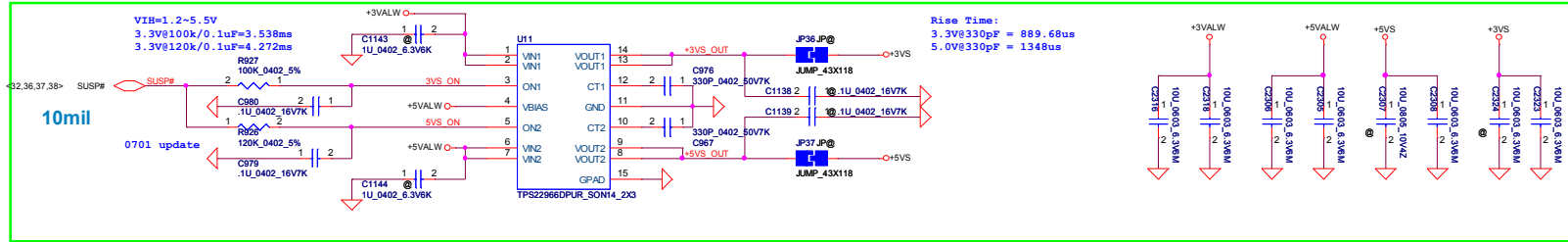


Security Classification		Compal Secret Data		Title	
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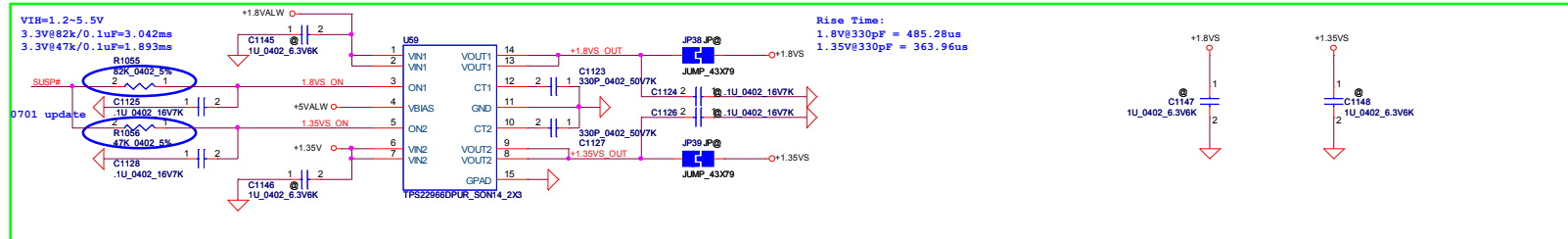




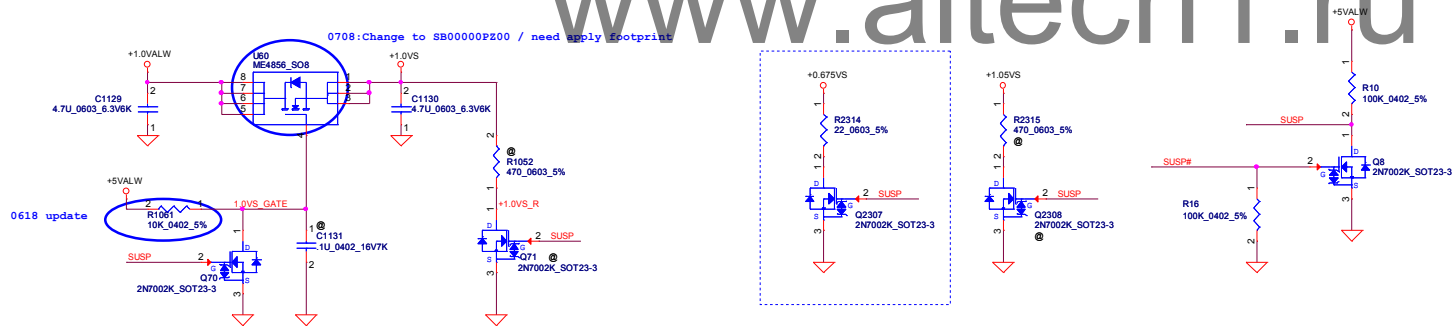
## +5VS and +3VS Switch



## +1.8VS and +1.35VS Switch



**+1.0VALW TO +1.0VS**



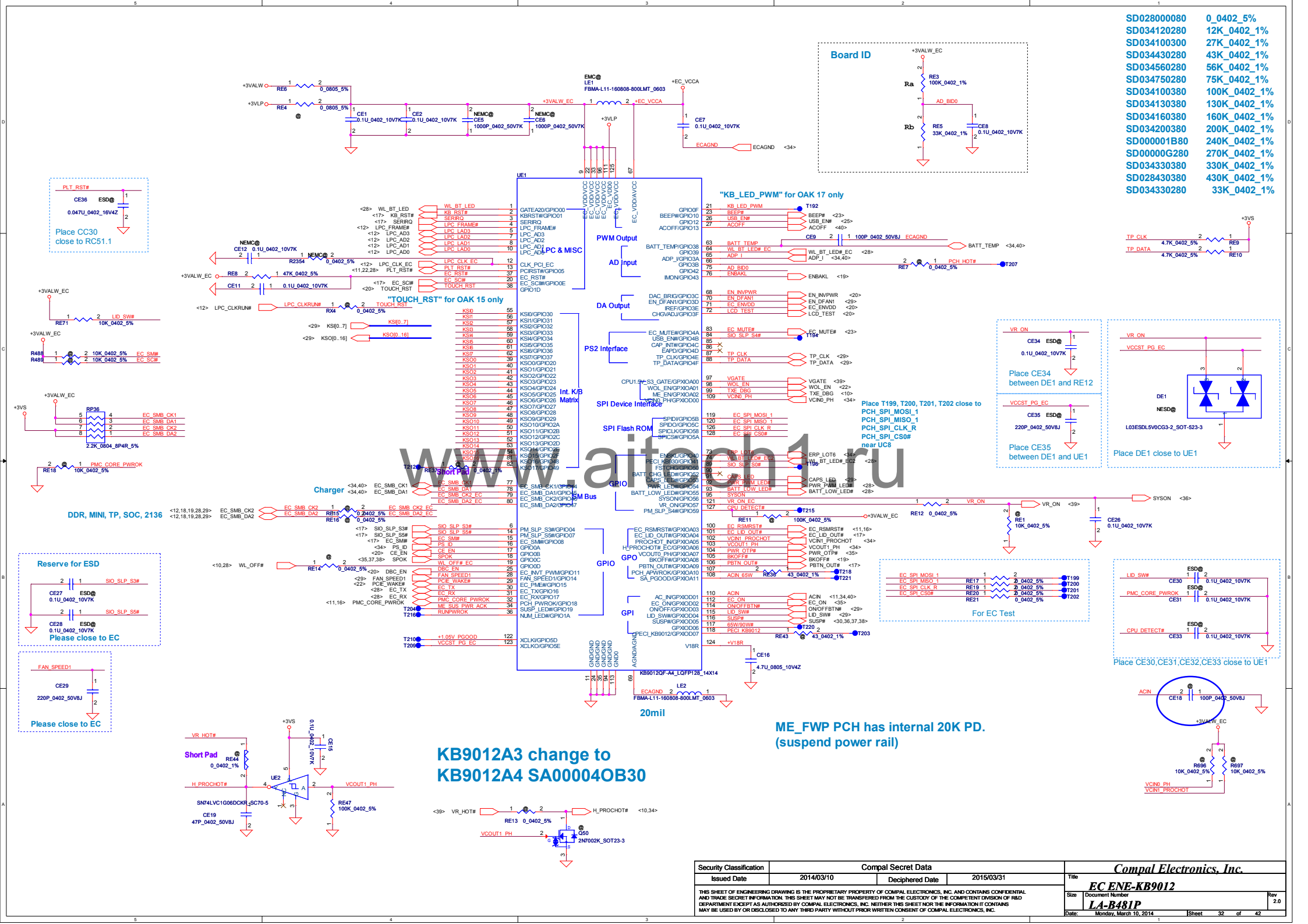
### For Intel S3 Power Reduction

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SLG3NB244VTR is for UMA by output 25M\*2, 32K\*1



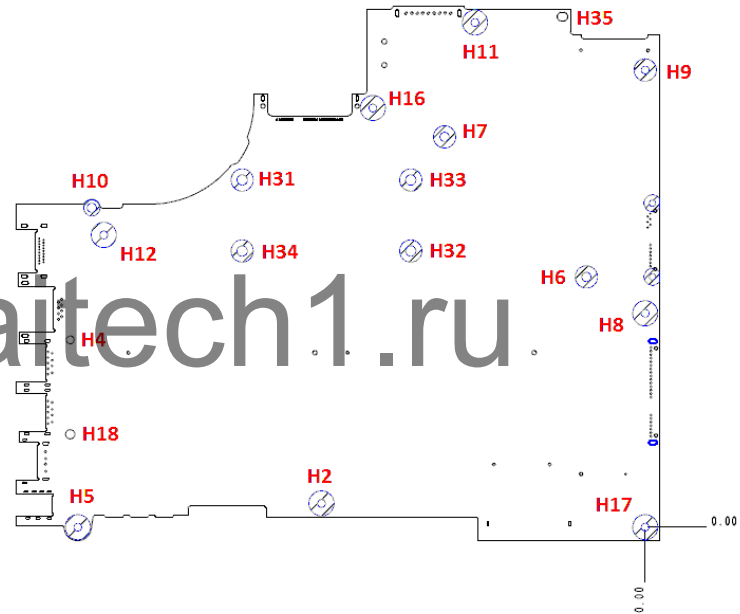
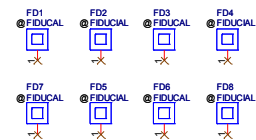
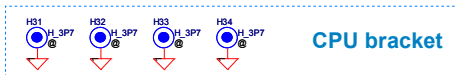
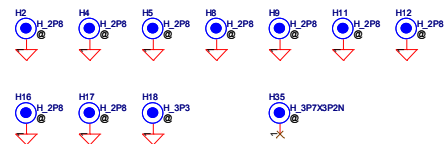
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Issued Date	2014/03/10	Deciphered Date	2015/03/31	<div>Title</div> <div>GCLK</div>			
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				<div>Date: Monday March 10, 2014</div> <div>Isheet 31 of 42</div>			



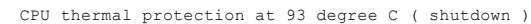
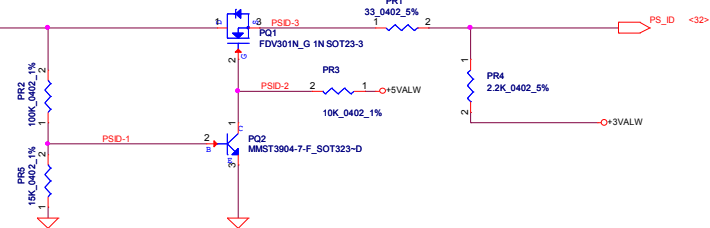
SD028000080	0_0402_5%
SD034120280	12K_0402_1%
SD034100380	27K_0402_1%
SD034403280	43K_0402_1%
SD034560280	56K_0402_1%
SD034750280	75K_0402_1%
SD034100380	100K_0402_1%
SD034130380	130K_0402_1%
SD034160380	160K_0402_1%
SD034200380	200K_0402_1%
SD00001B80	240K_0402_1%
SD0000G280	270K_0402_1%
SD034330380	330K_0402_1%
SD028430380	430K_0402_1%
SD034330280	33K_0402_1%

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Issued Date		Deciphered Date		EC ENE-KB9012	
2014/03/10		2015/03/31		Size	
				Document Number	
				LA-B481P	
				Date	
				Monday, March 10, 2014	
				Sheet	
				32 of 42	
				Rev	
				2.0	

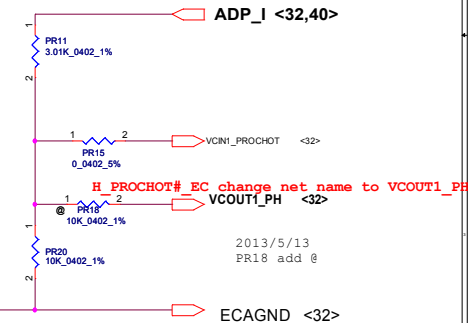
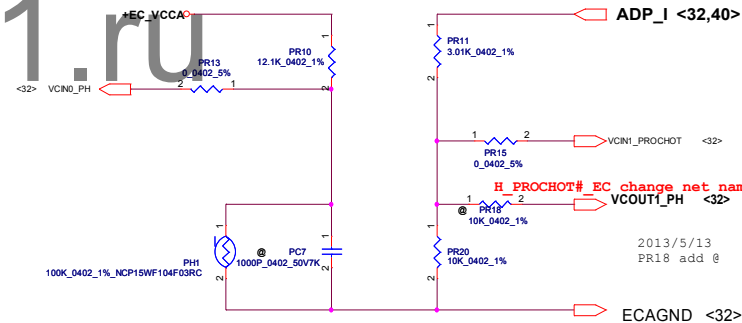
## Screw Hole



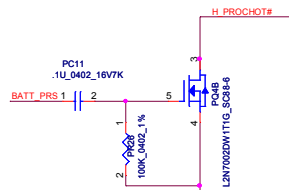
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Issued Date	2014/03/10	Deciphered Date	2015/03/31	Title	Screw Hole
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Delay adaptor OC H\_PROCHOT#  
2ms while hybrid power  
transition



if battery removed, adaptor only,  
then trigger the H\_PROCHOT#,  
keep @ in BOM since battery can not  
be removed by end user



Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> <b>P32-PWR-3.3VALWP/5VALWP</b>	
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				Custom	2.0
				Date: Monday, March 10, 2014         Sheet 35 of 42	

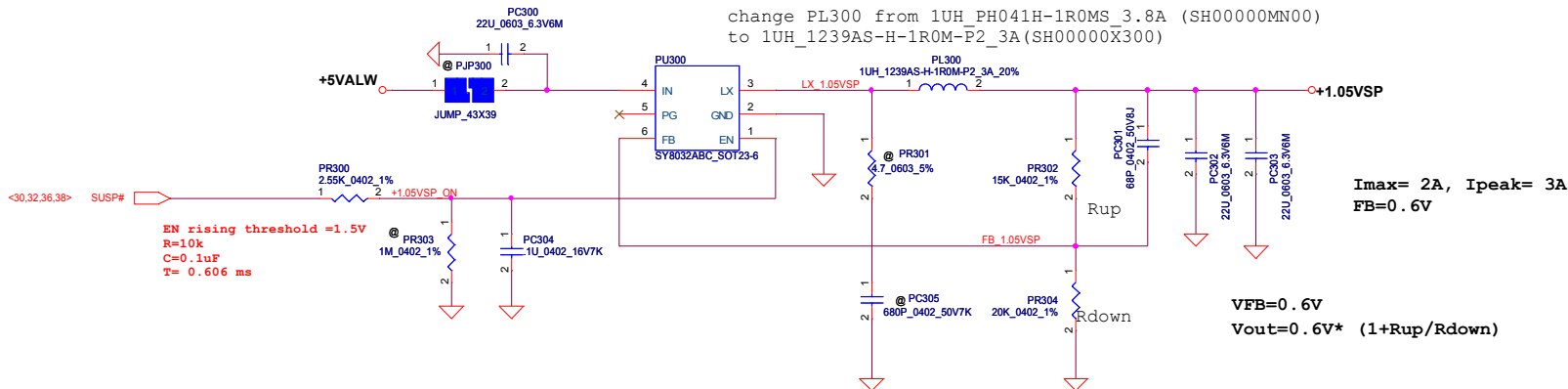
Mode	Level	+0.75VSP	VTTREF_1.5V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

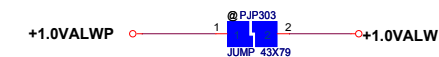
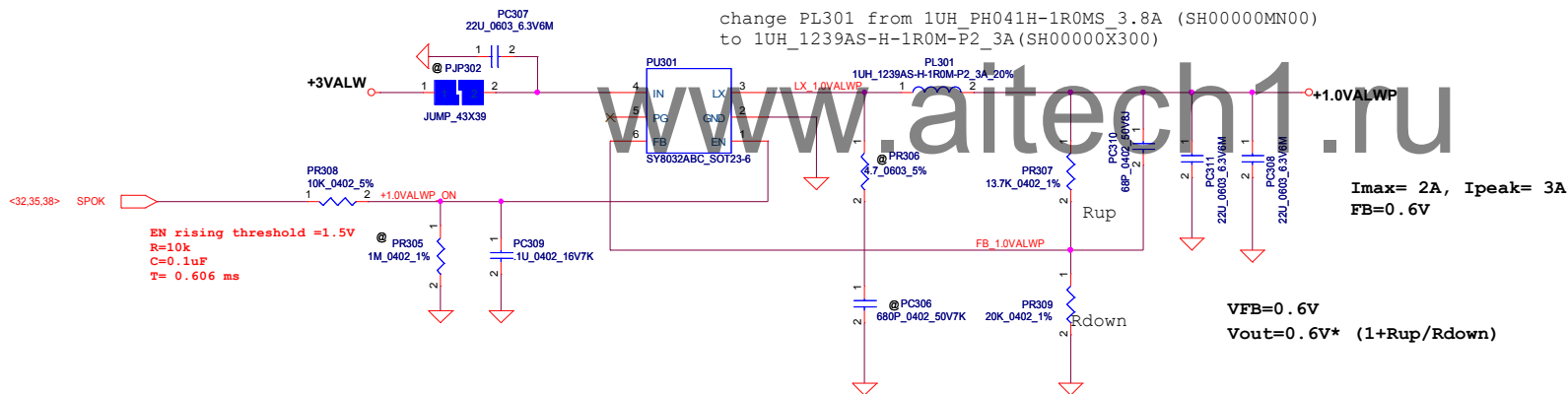
0.675Volt +/- 5%  
TDC 0.84A  
Peak Current 1.2A

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+1.05VSP  
TDC 0.7A  
Peak Current 1A  
OCP current 3.5A

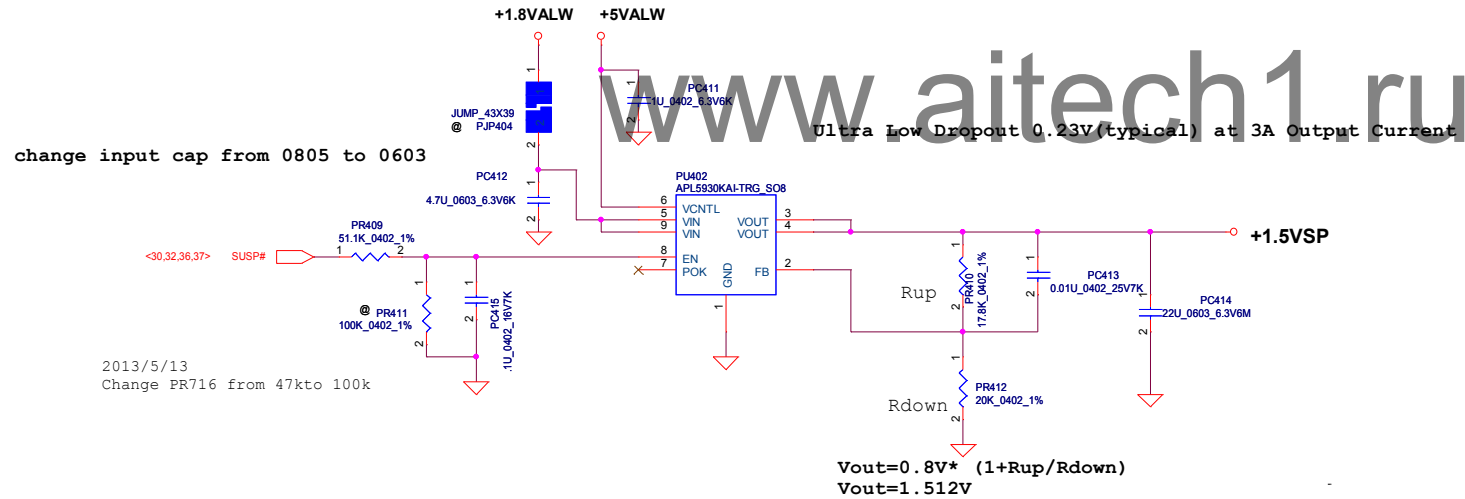
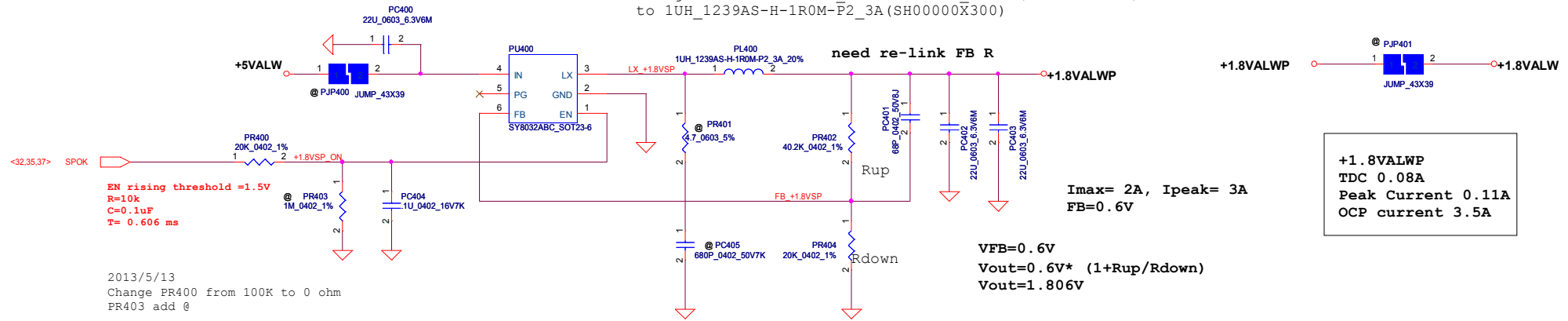


+1.0VALWP  
TDC 2.15A  
Peak Current 3.08A  
OCP current 3.5A

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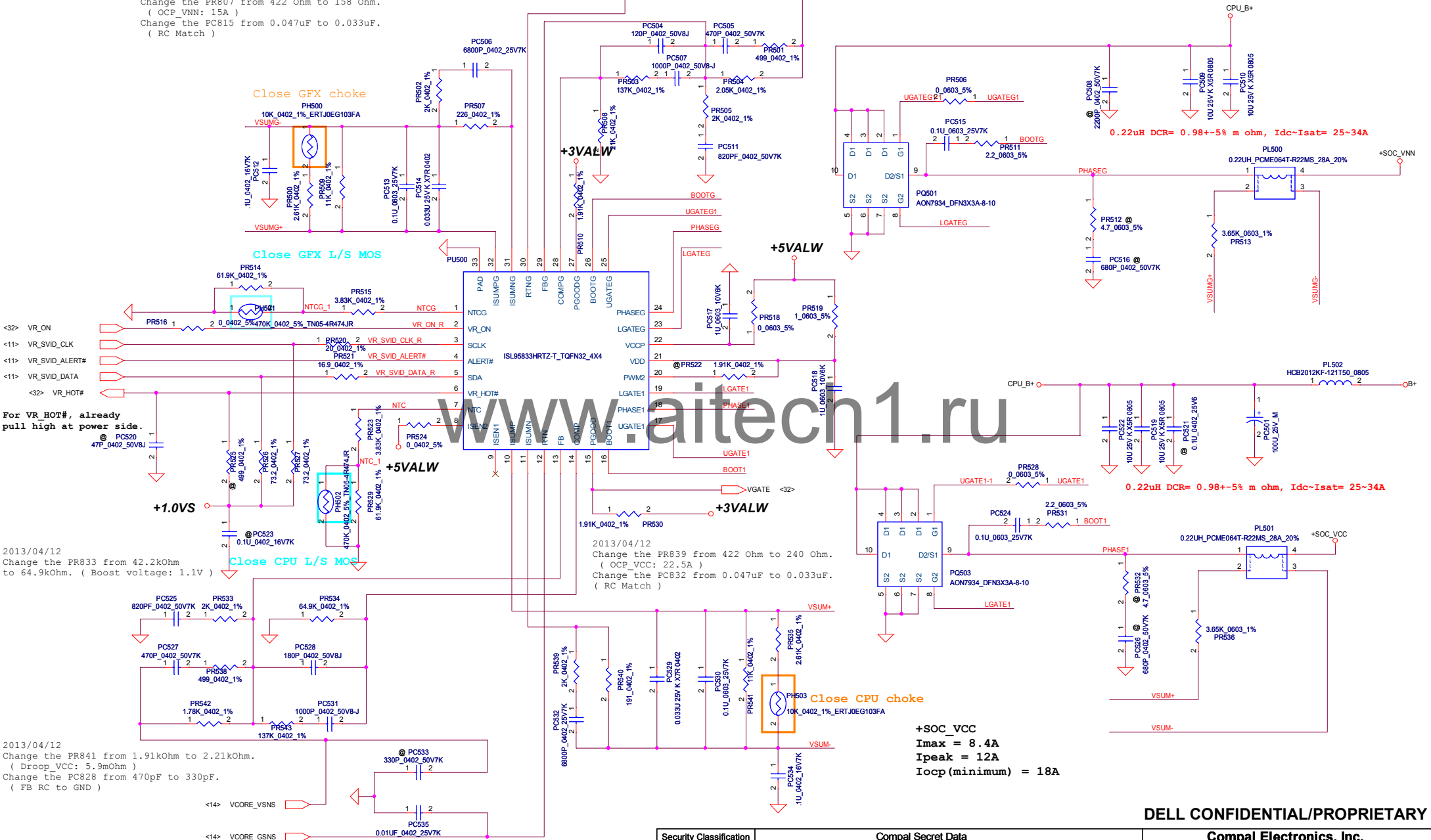
change PL400 from 1UH\_PH041H-1R0MS\_3.8A (SH00000MN00)  
to 1UH\_1239AS-H-1R0M-P2\_3A(SH00000X300)



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2013/04/12
Change the PR808 from @ to 21kOhm.
( Freq: 450kHz )
Change the PR807 from 422 Ohm to 158 Ohm.
( OCP_VNN: 15A )
Change the PC815 from 0.047uF to 0.033uF.
( RC Match )
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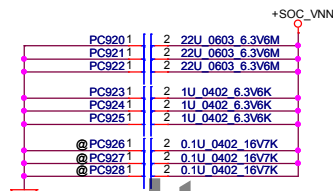
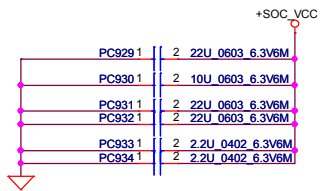
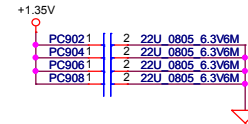
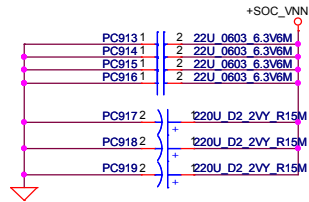
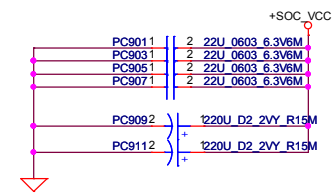
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### ***P38-PWR-CPU CORE***

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
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